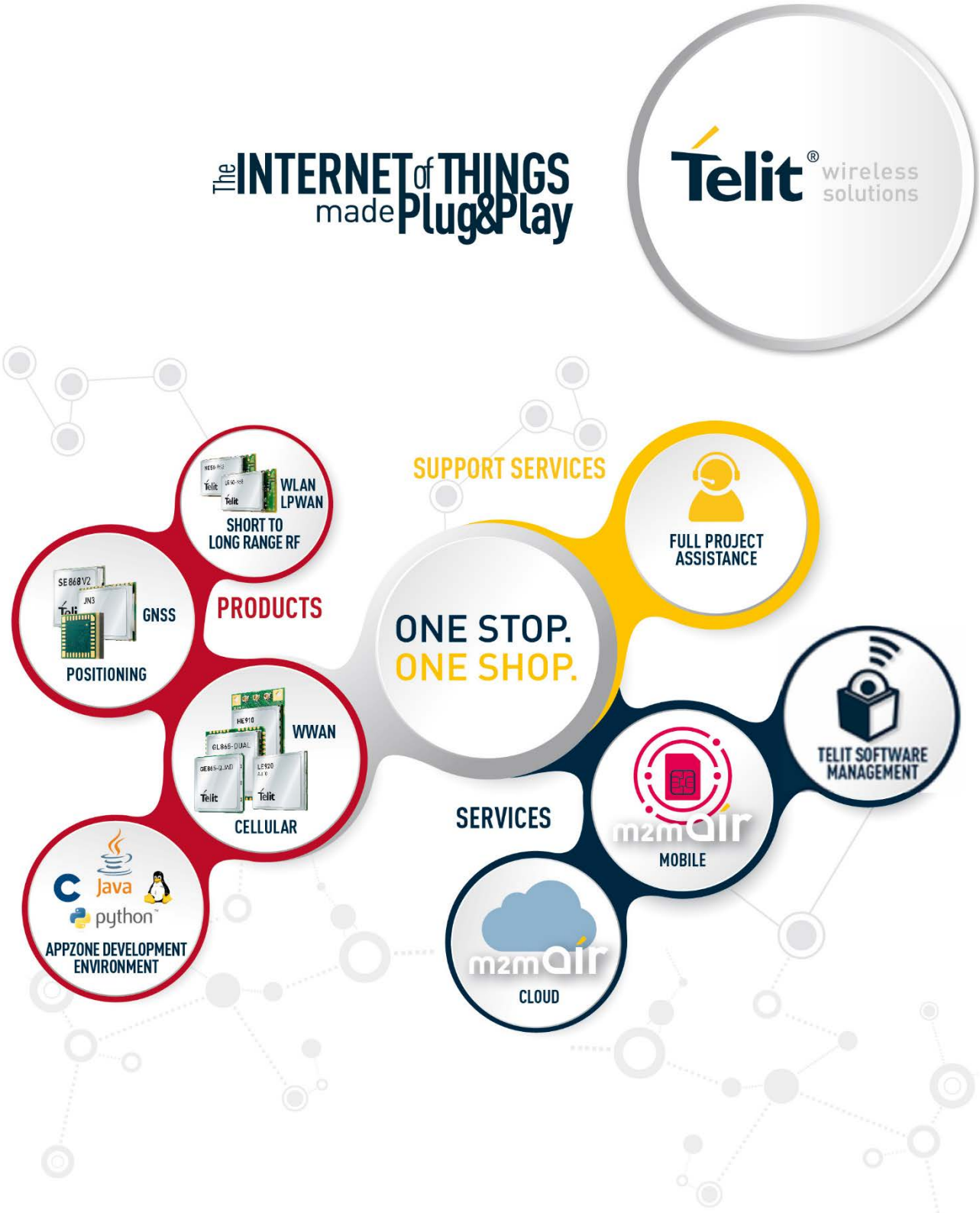

UE866 HARDWARE USER GUIDE

APPLICABILITY TABLE

PRODUCTS

- UE866-N3G
- UE866-EU

DISCLAIMER

LEGAL NOTICE

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CONTENTS

1 INTRODUCTION

1.1 Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit UE866 module.

1.2 Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our UE866 modules.

1.3 Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

TS-EMEA@telit.com

TS-AMERICAS@telit.com

TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4 List of acronyms

Acronym	Description
TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input
MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready
SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer

1.5 Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- Digital Voice Interface Application Note 80000NT10050A
- SPI Port Application Note 80000NT10053A
- SIM Holder Design Guides 80000NT10001a
- AT Commands Reference Guide 80378ST10091A
- Telit EVK2 User Guide 1vv0300704

2 OVERVIEW

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit UE866 module.
In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit UE866 module. For further hardware details that may not be explained in this document refer to the Telit UE866 Product Description document where all the hardware information is reported.

NOTICE:
(EN) The integration of the WCDMA **UE866** cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare WCDMA **UE866** all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des **UE866** WCDMA Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija WCDMA **UE866** modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo WCDMA **UE866** debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire WCDMA **UE866** dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי **UE866** עם המוצר.

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3 PINS ALLOCATION

3.1 Pin-out

Pin	Signal	I/O	Function	Type	Comment
USB HS 2.0 COMMUNICATION PORT					
E5	USB_D+	I/O	USB differential Data (+)	-	
E6	USB_D-	I/O	USB differential Data (-)	-	
D4	USB_VBUS	AI	Power sense for the internal USB transceiver.	-	
Asynchronous Serial Port (USIF0) - Prog. / Data + HW Flow Control					
B2	C109/DCD	O	Output for Data carrier detect signal (DCD) to DTE	CMOS 1.8V	
B3	C125/RING	O	Output for Ring indicator signal (RI) to DTE	CMOS 1.8V	
A3	C107/DSR	O	Output for Data set ready signal (DSR) to DTE	CMOS 1.8V	
A2	C108/DTR	I	Input for Data terminal ready signal (DTR) from DTE	CMOS 1.8V	
A1	C105/RTS	I	Input for Request to send signal (RTS) from DTE	CMOS 1.8V	
B1	C106/CTS	O	Output for Clear to send signal (CTS) to DTE	CMOS 1.8V	
A4	C103/TXD	I	Serial data input (TXD) from DTE	CMOS 1.8V	
A5	C104/RXD	O	Serial data output to DTE	CMOS 1.8V	
Asynchronous Auxiliary Serial Port (USIF1)					
C2	RXD_AUX /SPI_MISO	I O	Auxiliary UART (RX Data) SPI_MISO	CMOS 1.8V	
C1	TXD_AUX / SPI_MOSI	O I	Auxiliary UART (TX Data) SPI_MOSI	CMOS 1.8V	
SIM card interface					
C7	SIMVCC	-	External SIM signal – Power supply for the SIM	1.8 / 3V	
B7	SIMRST	O	External SIM signal – Reset	1.8 / 3V	
A7	SIMCLK	O	External SIM signal – Clock	1.8 / 3V	
A6	SIMIO	I/O	External SIM signal – Data I/O	CMOS 1.8	
X	SIMIN	I	Presence SIM input	1.8 / 3V	All GPI0 can be used
DIGITAL IO					
C5	GPIO_01 / DVI_WA0	I/O	GPIO01 Configurable GPIO	CMOS 1.8V	

			/ Digital Audio Interface (WA0)		
C6	GPIO_02 / JDR / DVI_RX	I/O	GPIO02 I/O pin / Jammer Detect Report / Digital Audio Interface (RX)	CMOS 1.8V	
D6	GPIO_03 / DVI_TX	I/O	GPIO03 GPIO I/O pin / Digital Audio Interface (TX)	CMOS 1.8V	
D5	GPIO_04 / DVI_CLK	I/O	GPIO04 Configurable GPIO Digital Audio Interface (CLK)	CMOS 1.8V	
B5	GPIO_05	I/O	GPIO05 Configurable GPIO	CMOS 1.8V	
B4	GPIO_06	I/O	GPIO06 Configurable GPIO / ALARM	CMOS 1.8V	
C4	GPIO_07	I/O	GPIO07 Configurable GPIO / STATLED	CMOS 1.8V	Alternate Function STAT LED
F11	SPI_CLK	I/O	SPI_CLK	CMOS 1.8V	
E11	SPI_SRDY	I/O	SPI_SRDY	CMOS 1.8V	
D11	SPI_MRDY	I/O	SPI_MRDY	CMOS 1.8V	
ADC and DAC					
F4	ADC_IN1	AI	Analog/Digital converter input	A/D	Accepted values 0 to 1.2V DC
E4	DAC_OUT	AO	Digital/Analog converter output	D/A	
RF SECTION					
G2	Antenna	I/O	Antenna pad – 50 Ω	RF	
Miscellaneous Functions					
F5	VRTC	AO	backup for the embedded RTC supply (1.8V)	-	
G4	RESET*	I	Reset Input	CMOS 1.8V	
G6	VAUX / PWRMON	O	1.8V stabilized output Imax=100mA / Power ON monitor	Power	
Power Supply					
E2	VBATT	-	Main power supply (Baseband)	Power	
E1	VBATT_PA	-	Main power supply (Radio PA)	Power	
D1	GND	-	Ground	Power	
F1	GND	-	Ground	Power	
G1	GND	-	Ground	Power	
D2	GND	-	Ground	Power	
F2	GND	-	Ground	Power	
C3	GND	-	Ground	Power	
E3	GND	-	Ground	Power	
F3	GND	-	Ground	Power	

G3	GND	-	Ground	Power
F6	GND	-	Ground	Power
A8	GND	-	Ground	Power
G8	GND	-	Ground	Power
A11	GND	-	Ground	Power
G11	GND	-	Ground	Power
RESERVED				
D3	RESERVED	-	RESERVED	
G5	RESERVED	-	RESERVED	
B6	RESERVED	-	RESERVED	
D7	RESERVED	-	RESERVED	
E7	RESERVED	-	RESERVED	
F7	RESERVED	-	RESERVED	
G7	RESERVED	-	RESERVED	
B8	RESERVED	-	RESERVED	
C8	RESERVED	-	RESERVED	
D8	RESERVED	-	RESERVED	
E8	RESERVED	-	RESERVED	
F8	RESERVED	-	RESERVED	
A9	RESERVED	-	RESERVED	
B9	RESERVED	-	RESERVED	
C9	RESERVED	-	RESERVED	
D9	RESERVED	-	RESERVED	
E9	RESERVED	-	RESERVED	
F9	RESERVED	-	RESERVED	
G9	RESERVED	-	RESERVED	
A10	RESERVED	-	RESERVED	
B10	RESERVED	-	RESERVED	
C10	RESERVED	-	RESERVED	
D10	RESERVED	-	RESERVED	
E10	RESERVED	-	RESERVED	
F10	RESERVED	-	RESERVED	
G10	RESERVED	-	RESERVED	
B11	RESERVED	-	RESERVED	
C11	RESERVED	-	RESERVED	

WARNING:

Reserved pins must not be connected

If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

PAD	Signal	Note
E2	VBATT	
E1	VBATT_PA	
D1, F1, G1, D2, F2, C3, E3, F3, G3, F6, A8, G8, A11, G11	GND	
G2	Antenna	
A4	C103/TXD	If not used should be connected to a Test Point
A5	C104/RXD	If not used should be connected to a Test Point
A1	C105/RTS	If not used should be connected to a Test Point
B1	C106/CTS	If not used should be connected to a Test Point
G6	VAUX / PWRMON	
G4	RESET*	
C1	TXD_AUX	If not used should be connected to a Test Point
C2	RXD_AUX	If not used should be connected to a Test Point
E5	USB D+	If not used should be connected to a Test Point or an USB connector
E6	USB D-	If not used should be connected to a Test Point or an USB connector
D4	USB_VBUS	If not used should be connected to a Test Point or an USB connector
C7	SIMVCC	
B7	SIMRST	
A7	SIMCLK	
A6	SIMIO	

RTS pin should be connected to the GND (on the module side) if flow control is not used.

The above pins are also necessary to debug the application when the module is assembled on it so we recommend connecting them also to dedicated test point.

3.1.1 LGA Pads Layout

TOP VIEW

	A	B	C	D	E	F	G
1	C105/RTS	C106/CTS	TX AUX	GND	VBATT_PA	GND	GND
2	C108/DTR	C109/DCD	RX AUX	GND	VBATT	GND	ANT
3	C107/DSR	C125/RING	GND	RFU	GND	GND	GND
4	C103/TXD	GPIO_06	GPIO_07	USB_VBUS	DAC_OUT	ADC_IN1	RESET*
5	C104/RXD	GPIO_05	GPIO_01	GPIO_04	USB_D+	VRTC	RESERVED
6	SIMIO	RESERVED	GPIO_02	GPIO_03	USB_D-	GND	VAUX/PWR MON
7	SIMCLK	SIMRST	SIMVCC	RESERVED	RESERVED	RESERVED	RESERVED
8	GND	RESERVED	RFU	RFU	RFU	RFU	GND
9	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
10	RESERVED	RESERVED	RESERVED	RESERVED	RFU	RESERVED	RESERVED
11	GND	RESERVED	RESERVED	SPI_MRDY	SPI_SRDY	SPI_CLK	GND

4 POWER SUPPLY

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performances, hence read carefully the requirements and the guidelines that will follow for a proper design.

4.1 Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfil the following requirements:

Power Supply	Value
Nominal Supply Voltage	3.8V
Normal Operating Voltage Range	3.40 V÷ 4.20 V
Extended Operating Voltage Range	3.10 V÷ 4.50 V

NOTE:
The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.
If the voltage drop is exceeding the limits it could cause a Power Off of the module.
The Power supply must be higher than 3.22 V to power on the module

Overshoot voltage (regarding MAX Extended Operating Voltage) and drop in voltage (regarding MIN Extended Operating Voltage) MUST never be exceeded;
The "Extended Operating Voltage Range" can be used only with completely assumption and application of the HW User guide suggestions.

4.2 Power Consumption

Mode	Average (mA)	Mode Description
Switched OFF	180uA	Module supplied but Switched Off
Idle mode (GSM/EDGE)		
AT+CFUN=1	19	Normal mode: full functionality of the module
AT+CFUN=4	16.5	Module is not registered on the network
AT+CFUN=5	1.2	Full functionality with power saving; DRX9 (1.3mA in case of DRX5).
Operative mode (GSM)		
CSD TX and RX Mode		**GSM Voice Call**
GSM 850/900 CSD PL5	220	
DCS1800/ PCS1900 CSD PL0	167	
GPRS 4TX+ 1RX		**GPRS Sending Data Mode**
GSM 850/900 PL5	580	
DCS1800/ PCS1900 PL0	438	
Idle mode (WCDMA)		
AT+CFUN=1	19	Normal mode: full functionality of the module
AT+CFUN=5	1.6 mA	Disabled TX and RX; DRX7
Operative mode (WCDMA)		
WCDMA Voice	175	WCDMA voice call (TX = 10dBm)
WCDMA HSDPA (22dBm)	490	WCDMA data call (Cat 8, TX = 22dBm)

NOTE:
The electrical design for the Power supply should be made ensuring it will be capable of a peak current output of at least 1 A.

4.3 General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout.

4.3.1 Electrical Design Guidelines

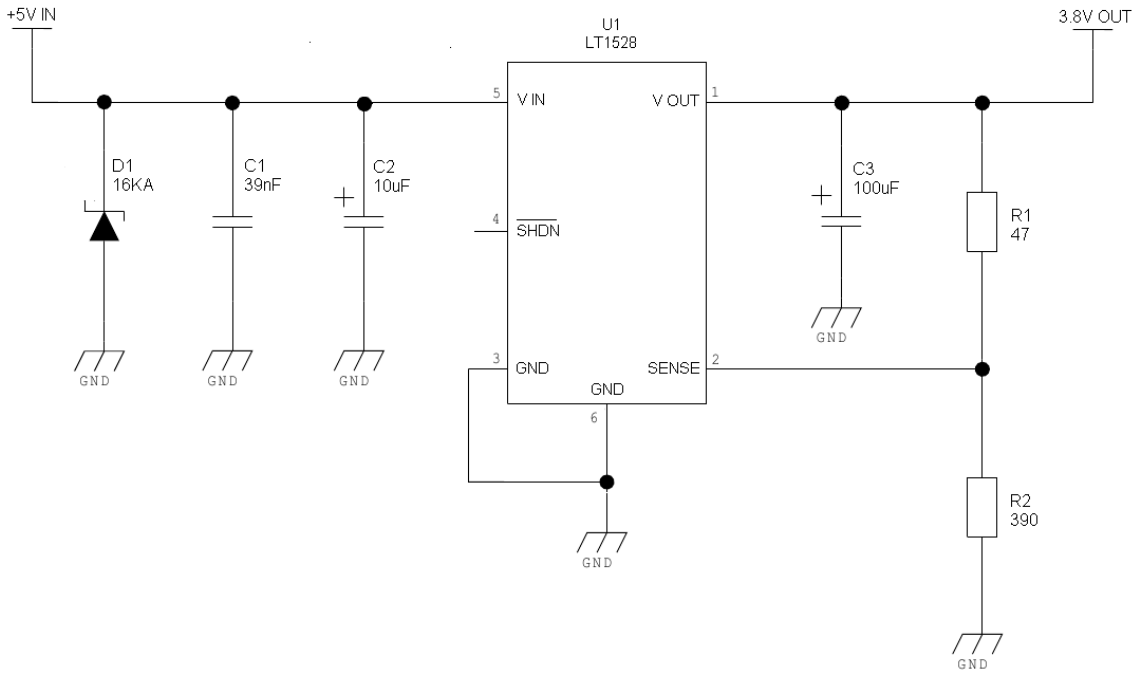
The electrical design of the power supply depends strongly from the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

4.3.1.1 *+5V Source Power Supply Design Guidelines*

- The desired output for the power supply is 3.8V, hence there's not a big difference between the input source and the desired output and a linear regulator can be used. A switching power supply will not be suited because of the low drop out requirements.
- When using a linear regulator, a proper heat sink shall be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the Module, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the UE866 from power polarity inversion. This can be the same diode as for spike protection.

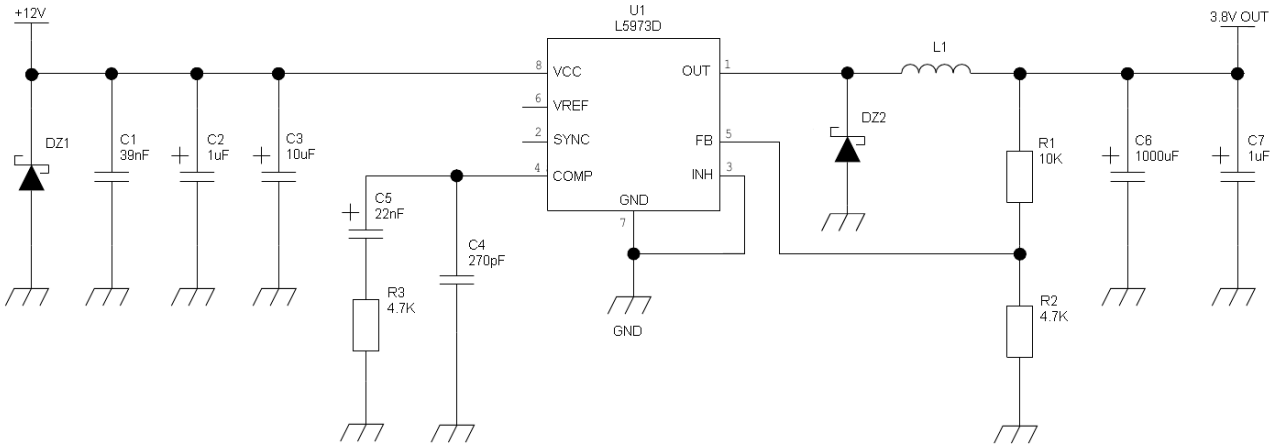
An example of linear regulator with 5V input is:



4.3.1.2 *+ 12V input Source Power Supply Design Guidelines*

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suited and shall not be used. A switching power supply will be preferable because of its better efficiency.
- When using a switching regulator, a 500kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case the frequency and Switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15,8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output is rated at least 10V.
- For Car applications a spike protection diode should be inserted close to the power input, in order to clean the supply from spikes.
- A protection diode should be inserted close to the power input, in order to save the UE866 from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the below schematic:



4.3.1.3 *Battery Source Power Supply Design Guidelines*

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V, hence a single 3.7V Li-Ion cell battery type is suited for supplying the power to the Telit UE866 module.

- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the UE866 from power polarity inversion. Otherwise the battery connector should be done in a way to avoid polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 2A; the suggested capacity is from 500mAh to 1000mAh.

WARNING:

The three cells Ni/Cd or Ni/MH 3,6 V Nom. battery types or 4V PB types ***MUST NOT BE USED DIRECTLY*** since their maximum voltage can rise over the absolute maximum voltage for the UE866 and damage it.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with UE866. Their use can lead to overvoltage on the UE866 and damage it. USE ONLY Li-Ion battery types.

4.3.1.4 *Thermal Design Guidelines*

The thermal design for the power supply heat sink should be done with the following specifications:

- Average current consumption during HSDPA transmission @PWR level max : 700 mA
- *Average current during idle:* 1.8 *mA*

Considering the very low current during idle, especially if Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

If we assume that the device stays into transmission for short periods of time (let's say few minutes) and then remains for a quite long time in idle (let's say one hour), then the power supply has always the time to cool down between the calls and the heat sink could be smaller than the calculated one for 700mA maximum RMS current, or even could be the simple chip package (no heat sink).
Moreover in the average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than the 700mA, being usually around 150mA.

In order to ensure a good thermal condition and to avoid overheating a ground plane as widest as possible according to application board and more vias to connect to module ground plane are recommended.
In this way, the generated heat will be mostly conducted to the ground plane under the UE866; you must ensure that your application can dissipate it.

NOTE:

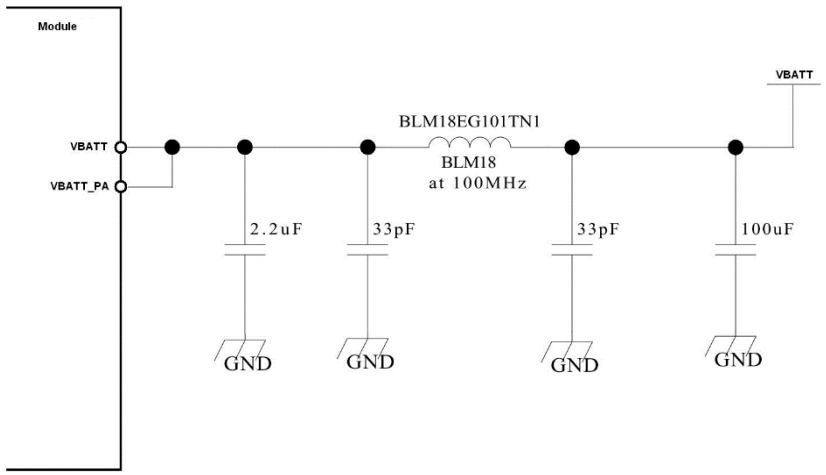
The average consumption during transmissions depends on the power level at which the device is requested to transmit by the network. The average current consumption hence varies significantly.

4.3.1.5 *Power Supply PCB layout Guidelines*

As seen on the electrical design guidelines the power supply shall have a low ESR capacitor on the output to cut the current peaks on the input to protect the supply from spikes The placement of this component is crucial for the correct working of the circuitry. A misplaced component can be useless or can even decrease the power supply performances.

- The Bypass low ESR capacitor must be placed close to the Telit UE866 power input pads or in the case the power supply is a switching type it can be placed close to the inductor to cut the ripple provided the PCB trace from the capacitor to the UE866 is wide enough to ensure a dropless connection even during an 1A current peak.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when an 1A current peak is absorbed.
- The PCB traces to the UE866 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur. This is for the same reason as previous point. Try to keep this trace as short as possible.
- To reduce the EMI due to switching, it is important to keep very small the mesh involved; thus the input capacitor, the output diode (if not embodied in the IC) and the regulator have to form a very small loop.This is done in order to reduce the radiated field (noise) at the switching frequency (100-500 kHz usually).
- A dedicated ground for the Switching regulator separated by the common ground plane is suggested.
- The placement of the power supply on the board should be done in such a way to guarantee that the high current return paths in the ground plane are not overlapped to any noise sensitive circuitry as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables should be kept separate from noise sensitive lines such as microphone/earphone cables.
- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.
  A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

The below figure shows the recommended circuit:



4.4 RTC Bypass out

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing having only RTC going on when all the other parts of the device are off.
To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery. NO Devices must be powered from this pin.

In order to keep the RTC active when VBATT is not supplied it is possible to back up the RTC section connecting a **backup circuit** to the related VRTC signal (pad F5 on module's Pinout).

For additional details on the Backup solutions please refer to the related application note (RTC Backup Application Note)

4.5 VAUX Power Output

A regulated power supply output is provided in order to supply small devices from the module. The signal is present on Pad G6 and it is in common with the PWRMON (module powered ON indication) function.
This output is always active when the module is powered ON.

The operating range characteristics of the supply are:

Item	Min	Typical	Max
Output voltage	1.77V	1.80V	1.83V
Output current	-	-	60mA
Output bypass capacitor (inside the module)		22uF	

NOTE:
The Output Current MUST never be exceeded; care must be taken when designing the application section to avoid having an excessive current consumption.
If the Current is exceeding the limits it could cause a Power Off of the module.

5 DIGITAL SECTION

5.1 Logic Levels Specification

ABSOLUTE MAXIMUM RATINGS – NOT FUNCTIONAL:

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.1V

OPERATING RANGE - INTERFACE LEVELS (1.8V CMOS):

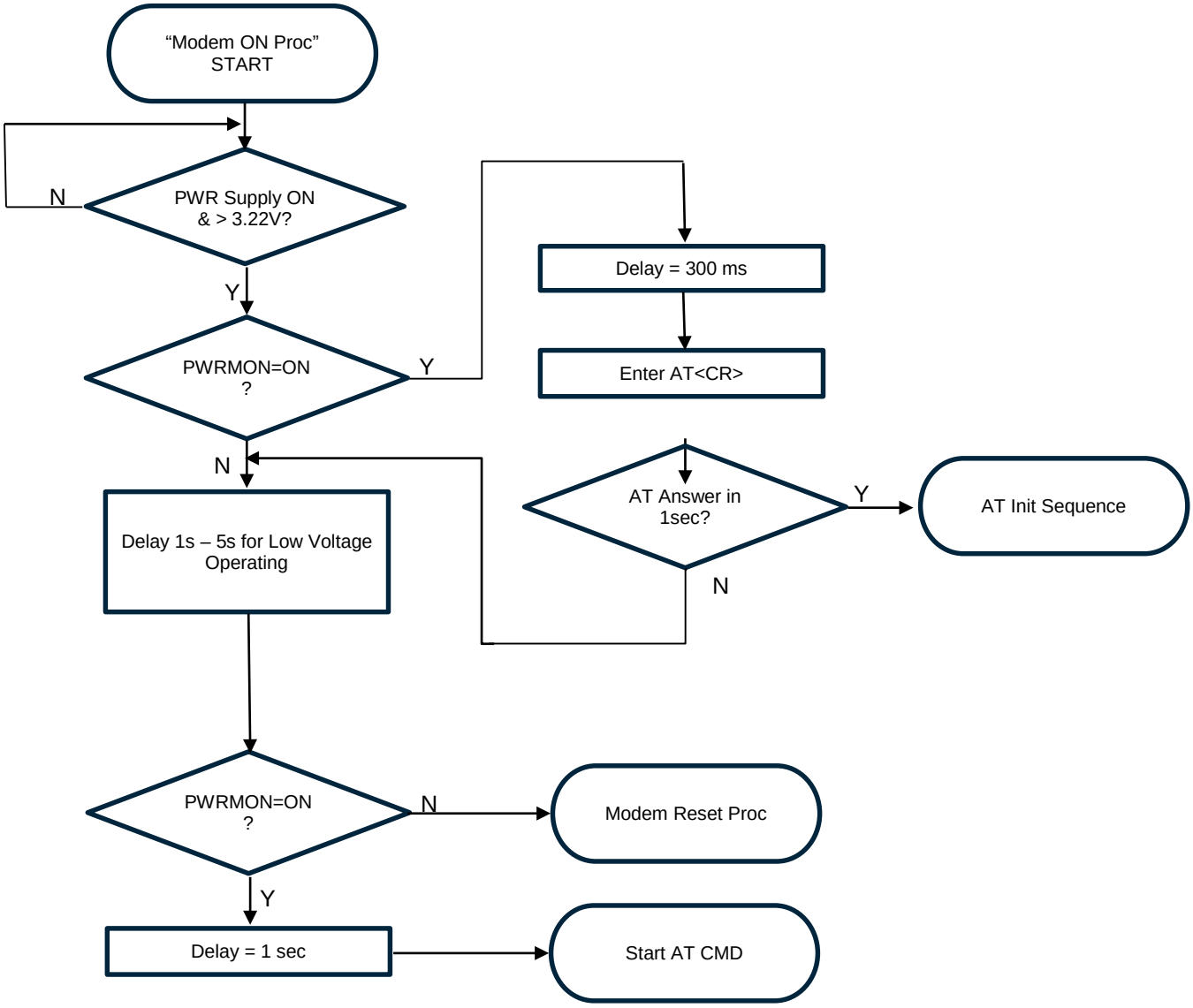
Parameter	Min	Max
Input high level	1.5V	1.9V
Input low level	0V	0.35V
Output high level	1.6V	1.9V
Output low level	0V	0.2V

CURRENT CHARACTERISTICS:

Parameter	AVG
Output Current	1mA
Input Current	1uA

5.2 Power on

The UE866 will automatically power on itself when VBATT & VBATT_PA are applied to the module. VAUX / PWRMON pin will be at the high logic level and the module can be considered fully operating after 5 seconds. The following flow chart shows the proper turn on procedure:

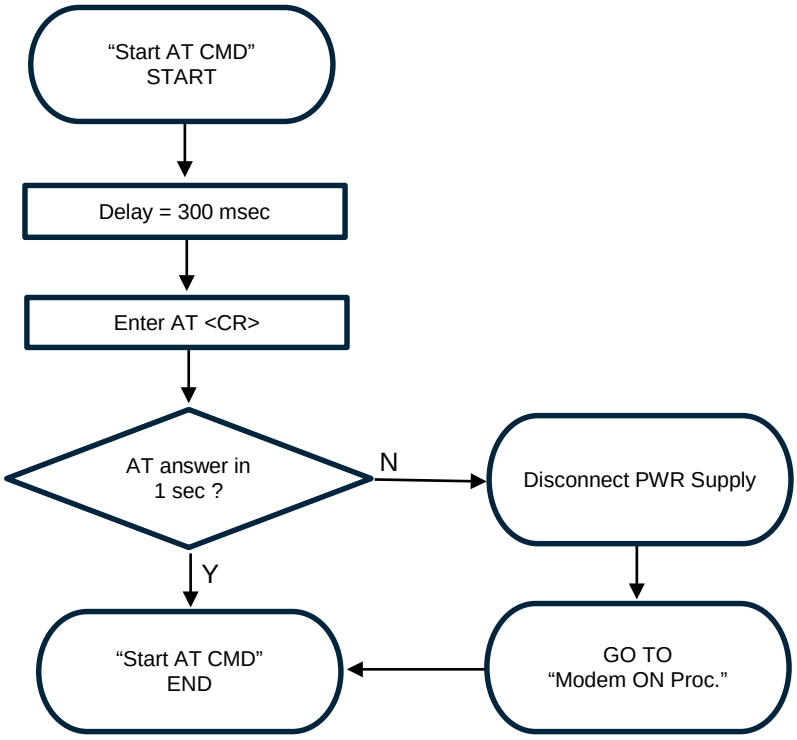


NOTE:

The power supply must be applied either at the same time on pins VBATT and VBATT_PA.

To guarantee a correct module's start-up please check that the Power Supply is with a level >3.22V within 21mS.

A flow chart showing the AT commands managing procedure is displayed below:



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE866 when the module is powered off or during an ON/OFF transition.

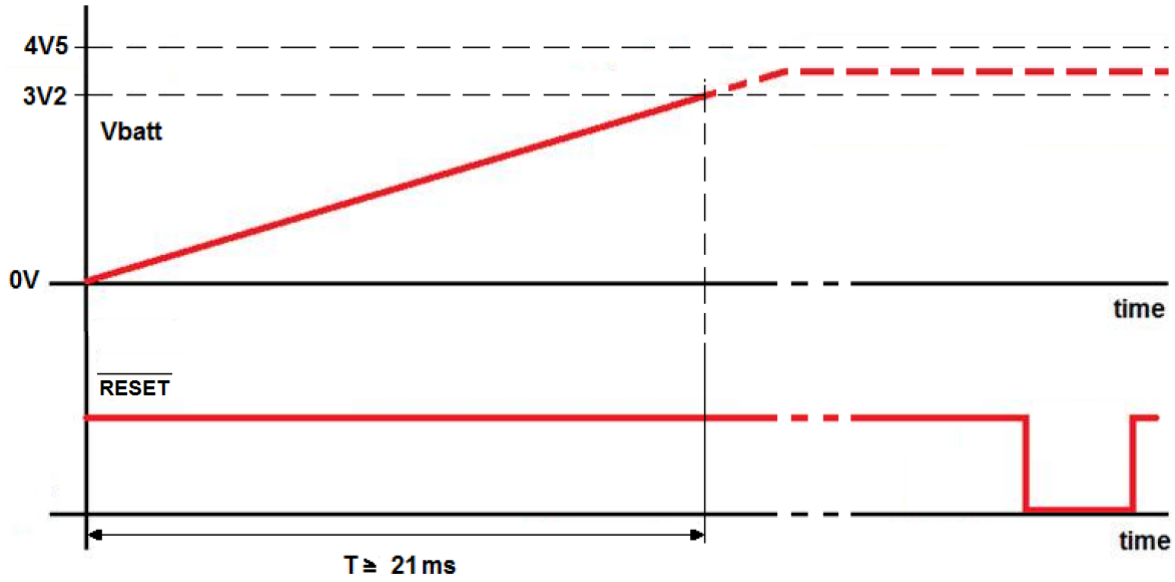
WARNING:

It is recommended to power on the module only after VBATT is higher than 3.22V.

The maximum rump up time for VBATT is 21mS.

In case this condition it is not satisfied you could use the HW_SHUTDOWN* line to recover it.

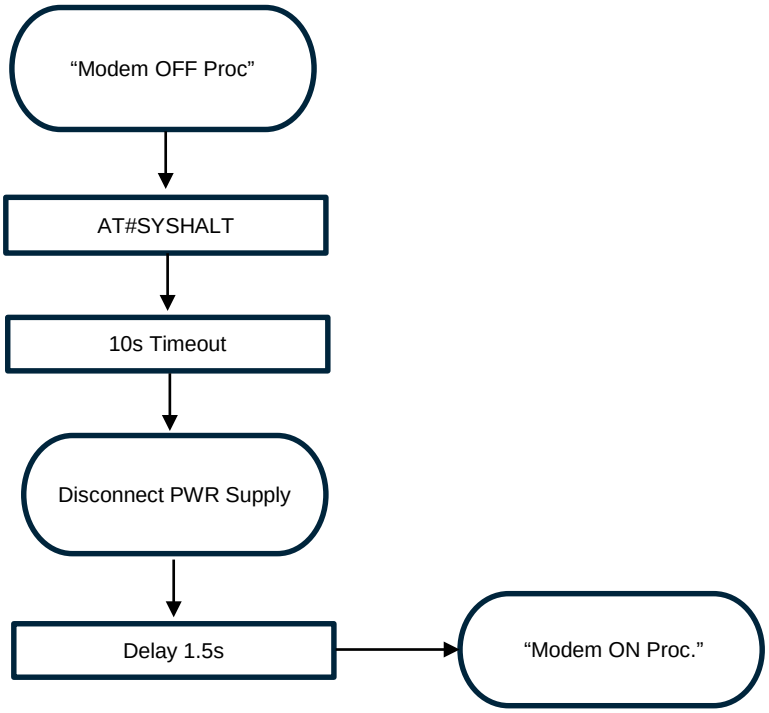
An example of this is described in the following diagram:



After RESET* is released the module will automatically power on itself.

5.3 Power off

The following flowchart shows the proper Turn-off procedure:



In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE866 when the module is powered off or during an ON/OFF transition.

5.4 Reset

To unconditionally reboot the UE866, the pad RESET* must be tied low for at least 200 milliseconds and then released.
The maximum current that can be drained from the RESET* pad is 0,15 mA.
The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stuck waiting for some network or SIM responses.

Do not use any pull up resistor on the RESET* line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the UE866 power regulator and improper functioning of the module.
The line RESET* must be connected only in open collector configuration; the transistor must be connected as close as possible to the RESET* pin.

The unconditional hardware restart must always be implemented on the boards and the software must use it as an emergency exit procedure.

PIN DESCRIPTION

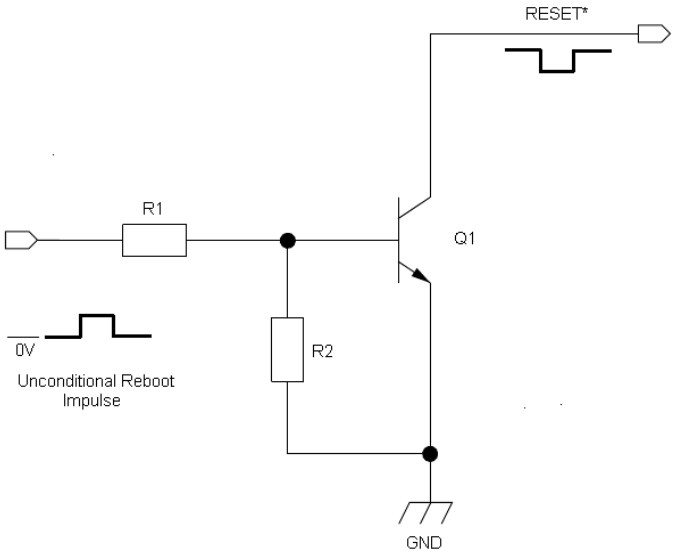
Signal	Function	I/O	PAD
RESET*	Unconditional Shutdown of the Module	I	G4

OPERATING LEVELS

Signal Status	Min	Max
RESET* Input high	1.5V	1.9V
RESET* Input Low	0V	0.35V

WARNING:
The hardware unconditional Shutdown must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure.

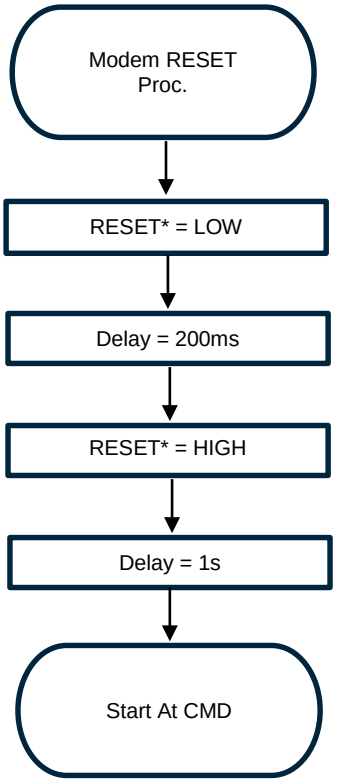
A typical circuit is the following:



NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE866 when the module is powered off or during an ON/OFF transition.

In the following flow chart is detailed the proper restart procedure:



NOTE:

Do not use any pull up resistor on the HW_SHUTDOWN* line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the UE866 power regulator and improper functioning of the module.

To proper power on again the module please refer to the related paragraph (“Power ON”)

The unconditional hardware shutdown must always be implemented on the boards and should be used only as an emergency exit procedure.

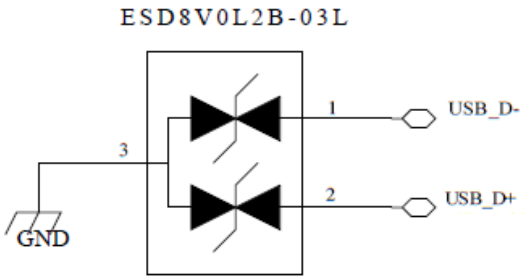
5.5 Communication ports

5.5.1 USB 2.0 HS

The UE866 includes one integrated universal serial bus (USB 2.0 HS) transceiver.
The following table is listing the available signals:

PAD	Signal	I/O	Function	Type	NOTE
E5	USB_D+	I/O	USB differential Data (+)	3.3V	
E6	USB_D-	I/O	USB differential Data (-)	3.3V	
D4	VUSB	AI	Power sense for the internal USB transceiver.	5V	Accepted range: 4.4V to 5.25V

The USB_DPLUS and USB_DMINUS signals have a clock rate of 480 MHz.
The signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized. The characteristic impedance value should be as close as possible to 90 Ohms differential.
In case there is a need to add an ESD protection, the suggested connection is the following:



NOTE:
VUSB pin should be disconnected before activating the Power Saving Mode.

5.5.2 SPI

The UE866 Module is provided by one SPI interface.

The SPI interface defines two handshake lines for flow control and mutual wake-up of the modem and the Application Processor: SRDY (slave ready) and MRDY (master ready).

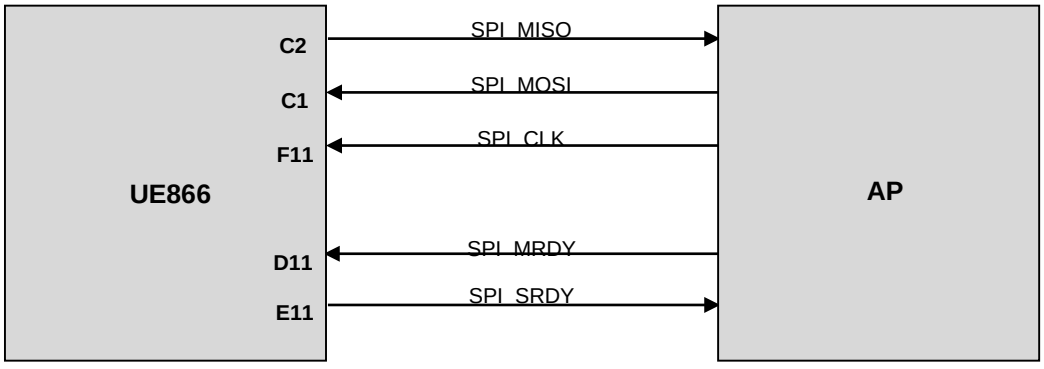
The AP has the master role, that is, it supplies the clock.

The following table is listing the available signals:

PAD	Signal	I/O	Function	Type	NOTE
C1	SPI_MOSI	I	SPI MOSI	CMOS 1.8V	Shared with TX_AUX
C2	SPI_MISO	O	SPI MISO	CMOS 1.8V	Shared with RX_AUX
F11	SPI_CLK	I	SPI Clock	CMOS 1.8V	
D11	SPI_MRDY	I	SPI_MRDY	CMOS 1.8V	
E11	SPI_SRDY	O	SPI_SRDY	CMOS 1.8V	

NOTE:
Due to the shared functions, when the SPI port is used, it is not possible to use the AUX_UART port.

5.5.2.1 *SPI Connections*



5.5.3 Serial Ports

The UE866 module is provided with by 2 Asynchronous serial ports:

- MODEM SERIAL PORT 1 (Main)
- MODEM SERIAL PORT 2 (Auxiliary)

Several configurations can be designed for the serial port on the OEM hardware, but the most common are:

- RS232 PC com port
- microcontroller UART @ 1.8V (Universal Asynchronous Receive Transmit)
- microcontroller UART @ 5V or other voltages different from 1.8V

Depending from the type of serial port on the OEM hardware a level translator circuit may be needed to make the system work.
On the UE866 the ports are CMOS 1.8.

5.5.3.1 *MODEM SERIAL PORT 1 (USIF0)*

The serial port 1 on the UE866 is a +1.8V UART with all the 7 RS232 signals.
It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

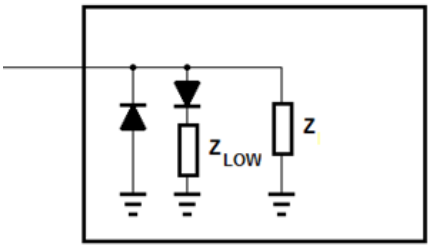
The following table is listing the available signals:

RS232 Pin	Signal	Pad	Name	Usage
1	C109/DCD	B2	Data Carrier Detect	Output from the UE866 that indicates the carrier presence
2	C104/RXD	A5	Transmit line *see Note	Output transmit line of UE866 UART
3	C103/TXD	A4	Receive line *see Note	Input receive of the UE866 UART
4	C108/DTR	A2	Data Terminal Ready	Input to the UE866 that controls the DTE READY condition
5	GND	D1, F1, G1, D2, F2, C3, E3, F3, G3, F6, A8, G8, A11, G11	Ground	Ground
6	C107/DSR	A2	Data Set Ready	Output from the UE866 that indicates the module is ready
7	C106/CTS	A1	Clear to Send	Output from the UE866 that controls the Hardware flow control
8	C105/RTS	B1	Request to Send	Input to the UE866 that controls the Hardware flow control
9	C125/RING	B3	Ring Indicator	Output from the UE866 that indicates the incoming call condition

The following table shows the typical input value of internal pull-up resistors for RTS, DTR and TXD input lines and in all module states:

STATE	RTS DTR TXD	
		Pull up tied to
ON	5K to 12K	1V8
OFF	Schottky diode	
RESET	Schottky diode	
POWER SAVING	5K to 12K	1V8

The input line ON_OFF and HW_SHDN state can be treated as in picture below



NOTE:
According to V.24, some signal names are referred to the application side, therefore on the UE866 side these signal are on the opposite direction:
TXD on the application side will be connected to the receive line (here named C103/TXD)
RXD on the application side will be connected to the transmit line (here named C104/RXD)

For a minimum implementation, only the TXD, RXD lines can be connected, the other lines can be left open provided a software flow control is implemented.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE866 when the module is powered off or during an ON/OFF transition.

5.5.3.2 *MODEM SERIAL PORT 2 (USIF1)*

The secondary serial port on the UE866 is a CMOS1.8V with only the RX and TX signals.
The signals of the UE866 serial port are:

PAD	Signal	I/O	Function	Type	NOTE
C1	TX_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 1.8V	Shared with SPI_MOSI
C2	RX_AUX	I	Auxiliary UART (RX Data from DTE)	CMOS 1.8V	Shared with SPI_MISO

NOTE:
Due to the shared pins, when the Modem Serial port is used, it is not possible to use the SPI functions.

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE866 when the module is powered off or during an ON/OFF transition.

5.5.3.3 *RS232 LEVEL TRANSLATION*

In order to interface the UE866 with a PC com port or a RS232 (EIA/TIA-232) application a level translator is required. This level translator must:

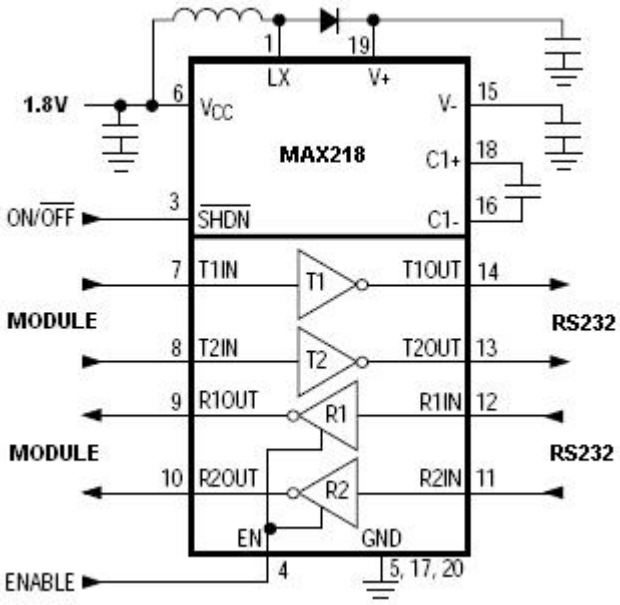
- invert the electrical signal in both directions;
- Change the level from 0/1.8V to +15/-15V.

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.
The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).
By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.
In order to translate the whole set of control lines of the UART you will need:

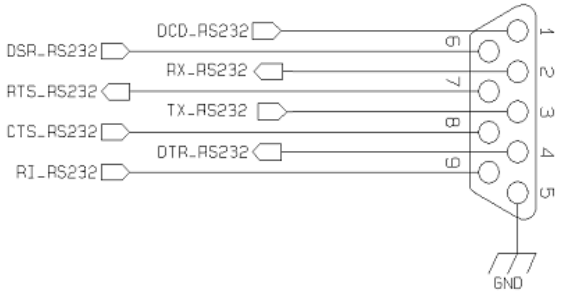
- 5 drivers
- 3 receivers

An example of RS232 level adaptation circuitry could be done using a MAXIM transceiver (MAX218)

In this case the chipset is capable to translate directly from 1.8V to the RS232 levels (Example done on 4 signals only).



The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



5.6 General Purpose I/O

The UE866 module is provided by a set of Configurable Digital Input / Output pins (CMOS 1.8V)
Input pads can only be read; they report the digital value (high or low) present on the pad at the read time.
Output pads can only be written or queried and set the value of the pad output.
An alternate function pad is internally controlled by the UE866 firmware and acts depending on the function implemented.

The following table shows the available GPIO on the UE866:

PAD	Signal	I/O	Drive Strength	Default State	NOTE
C5	GPIO_01	I/O	**1** mA	INPUT	Alternate function Digital Audio Interface (WA0
C6	GPIO_02	I/O	**1** mA	INPUT	Alternate functions Jammer Detect Report / Digital Audio Interface (RX)
D6	GPIO_03	I/O	**1** mA	INPUT	Alternate function Digital Audio Interface (TX)
D5	GPIO_04	I/O	**1** mA	INPUT	Alternate function TX Disable / Digital Audio Interface (CLK)
B5	GPIO_05	I/O	**1** mA	INPUT	
B4	GPIO_06	I/O	**1** mA	INPUT	Alternate function ALARM
C4	GPIO_07	I/O	**1** mA	INPUT	Alternate function STAT LED

NOTE:
The internal GPIO's pull up/pull down could be set to the preferred status for the application using the AT#GPIO command.
Please refer for the AT Commands User Guide for the detailed command Syntax.

WARNING:
During power up the GPIOs may be subject to transient glitches.

Also the UART's control flow pins can be usable as GPIO:

PAD	Signal	I/O	Input/output current	Default State	ON_OFF state	Reset State	NOTE
B2	GPO_A	O	1uA/1mA	INPUT	0	0	Alternate function C109/DCD
B3	GPO_B	O	1uA/1mA	INPUT	0	0	Alternate function C125/RING
A3	GPO_C	O	1uA/1mA	INPUT	0	0	Alternate function C107/DSR
A2	GPI_E	I	1uA/1mA	INPUT	0	0	Alternate function C108/DTR
A1	GPI_F	I	1uA/1mA	INPUT	0	0	Alternate function C105/RTS
B1	GPO_D	O	1uA/1mA	INPUT	0	0	Alternate function C106/CTS

5.6.1 Using a GPIO as INPUT

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47K pull up to 1.8V.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the UE866 when the module is powered off or during an ON/OFF transition.

The V_AUX / PWRMON pin can be used for input pull up reference or/and for ON monitoring.

5.6.2 Using a GPIO as OUTPUT

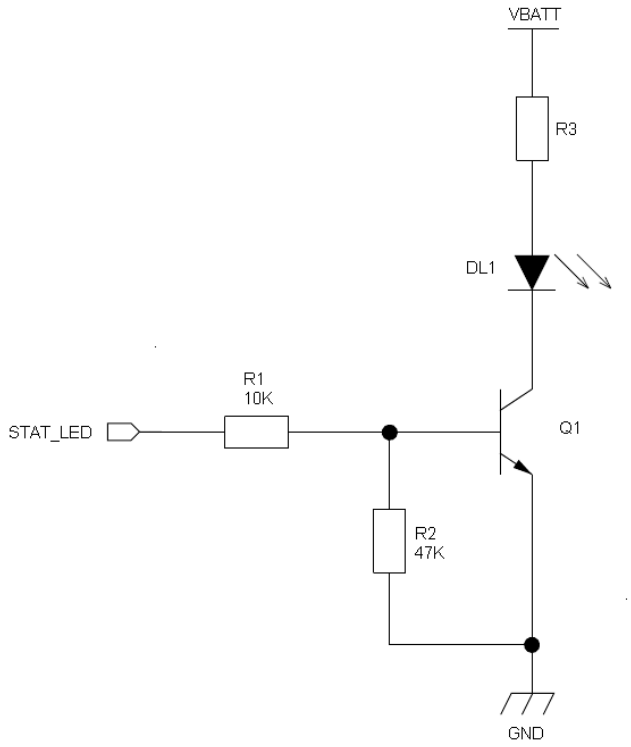
The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

5.6.3 Indication of network service availability

The STAT_LED pin status shows information on the network service availability and Call status.
The function is available as alternate function of GPIO_07 (to be enabled using the AT#GPIO=7,0,2 command).
In the UE866 modules, the STAT_LED needs an external transistor to drive an external LED.
Therefore, the status indicated in the following table is reversed with respect to the pin status.

Device Status	Led Status
Device off	Permanently off
Not Registered	Permanently on
Registered in idle	Blinking 1sec on + 2 sec off
Registered in idle + power saving	It depends on the event that triggers the wakeup (In sync with network paging)
Voice Call Active	Permanently on
Dial-Up	Blinking 1 sec on + 2 sec off

A schematic example could be:



5.6.4 SIMIN Detection

All the GPIO pins can be used as SIM DETECT input. The AT Command used to enable the function is:

AT#SIMINCFG

Use the AT command **AT#SIMDET=2** to enable the SIMIN detection
Use the AT command **AT&W0** and **AT&P0** to store the SIMIN detection **in the common profile.**

NOTE:
Don't use the SIM IN function on the same pin where the GPIO function is enabled and vice versa!

5.7 External SIM Holder

Please refer to the related User Guide (SIM Holder Design Guides, 80000NT10001a).

5.8 ADC Converter

The UE866 is provided by one AD converter. It is able to read a voltage level in the range of 0÷1.2 volts applied on the ADC pin input, store and convert it into 10 bit word.
The input line is named as **ADC_IN1** and it is available on Pad **F4**

The following table is showing the ADC characteristics:

Item	Min	Typical	Max	Unit
Input Voltage range	0	-	1.2	Volt
AD conversion	-	-	10	bits
Input Resistance	1	-	-	Mohm
Input Capacitance	-	1	-	pF

The ADC could be controlled using an AT command.
The command is ***AT#ADC=1,2***
The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

5.9 DAC Converter

The UE866 provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on pin **E4** of the UE866.

The on board DAC is a 10 bit converter, able to generate an analogue value based on a specific input in the range from 0 up to 1023. However, an external low-pass filter is necessary

The following table is showing the ADC characteristics:

Item	Min	Max	Unit
Voltage range (filtered)	0	1.8	Volt
Range	0	1023	Steps

The precision is 10 bits so, if we consider that the maximum voltage is 2V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = (2 *value) / 1023

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

5.9.1 Enabling DAC

An *AT command* is available to use the DAC function.

The command is: **AT#DAC= [**<*enable*> **[,** <*value*>**]]**

<value> - scale factor of the integrated output voltage (0..1023 - 10 bit precision)

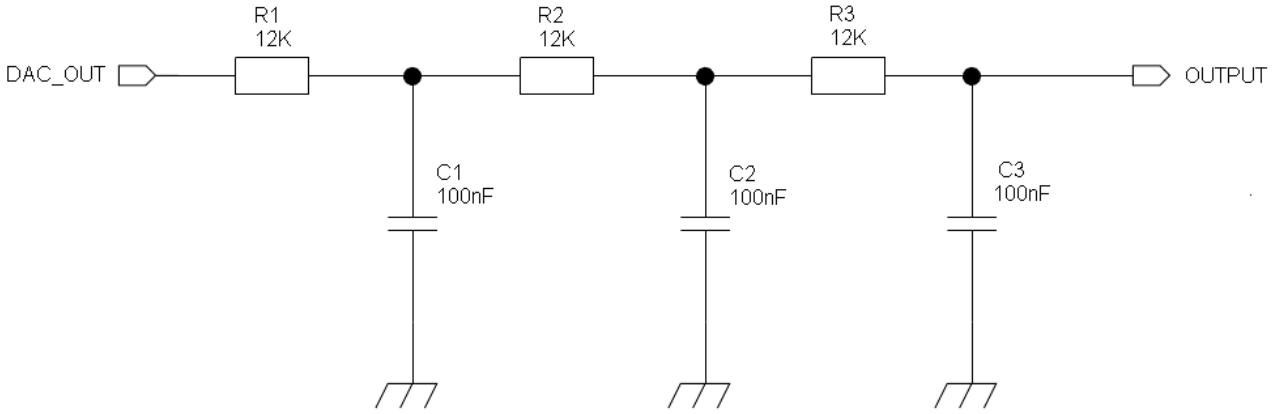
it must be present if ***<enable>=1***

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

NOTE:

The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.

5.9.2 LOW Pass filter Example



6 RF SECTION

6.1 Bands Variants

The following table is listing the supported Bands:

Product	Supported 2G bands
UE866-N3G	-
UE866-EU	GSM900, DCS1800

Product	Supported 3G bands
UE866-N3G	FDD B2, B5
UE866-EU	FDD B1, B8

6.2 TX Output Power

Band	Power Class
GSM 900	Class 4 (2W)
DCS 1800	Class 1 (15W)
FDD B1, B8	Class 3 (0.25W)
FDD B2, B5	Class 3 (0.25W)

6.3 RX Sensitivity

Band	Sensitivity
GSM 900	-109dBm
DCS 1800	-110dBm
FDD B1, B8	-111dBm
FDD B2, B5	-110dBm

6.4 Antenna Requirements

The antenna connection and board layout design are the most important aspect in the full product design as they strongly affect the product overall performances, hence read carefully and follow the requirements and the guidelines for a proper design.
The antenna and antenna transmission line on PCB for a Telit UE866 device shall fulfil the following requirements:

Item	Value
Frequency range	Depending by frequency band(s) provided by the network operator, the customer shall use the most suitable antenna for that/those band(s)
Bandwidth	80 MHz in GSM900 170 MHz in DCS
Bandwidth (WCDMA)	70 MHz in WCDMA Band V 140 MHz in WCDMA Band II 250 MHz in WCDMA B I 80 MHz in WCDMA B VIII
Impedance	50 ohm
Input power	>33 dBm (2W) peak power in GSM >24dBm Average power in WCDMA
VSWR absolute max	≤ 10:1 (limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (limit to fulfill all regulatory requirements)

6.4.1 PCB design guidelines

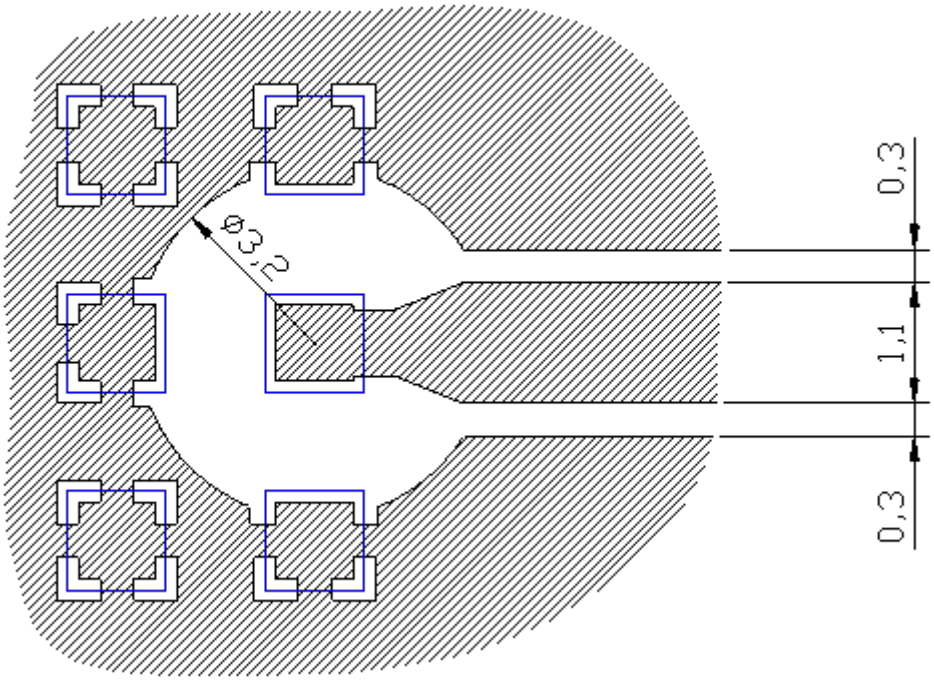
When using the UE866, since there's no antenna connector on the module, the antenna must be connected to the UE866 antenna pad by means of a transmission line implemented on the PCB.
In the case the antenna is not directly connected at the antenna pad of the UE866, then a PCB line is needed in order to connect with it or with its connector.
This transmission line shall fulfil the following requirements:

Item	Value
Characteristic Impedance	50 ohm
Max Attenuation	0,3 dB
Coupling	Coupling with other signals shall be avoided
Ground Plane	Cold End (Ground Plane) of antenna shall be equipotential to the UE866 ground pins

The transmission line should be designed according to the following guidelines:

- Ensure that the antenna line impedance is 50 ohm;
- Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0,3 dB;
- Antenna line must have uniform characteristics, constant cross section; avoid meanders and abrupt curves;
- Keep, if possible, one layer of the PCB used only for the Ground plane;
- Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
- The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias every 2mm at least;
- Place EM noisy devices as far as possible from UE866 antenna line;
- Keep the antenna line far away from the UE866 power supply lines;
- If you have EM noisy devices around the PCB hosting the UE866, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
- If you don't have EM noisy devices around the PCB of UE866, by using a micro strip on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one;

The following image is showing the suggested layout for the Antenna pad connection:



6.4.2 PCB Guidelines in case of FCC Certification

In the case FCC certification is required for an application using UE866-N3G, according to FCC KDB 996369 for modular approval requirements, the transmission line has to be similar to that implemented on UE866 interface board and described in the following chapter.

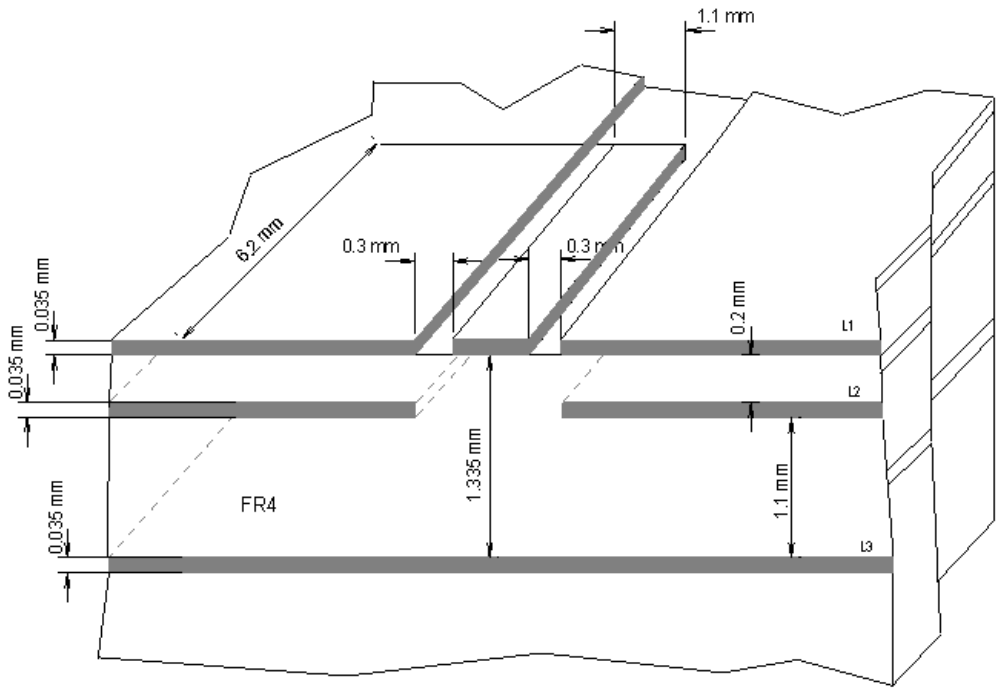
6.4.2.1 *Transmission line design*

During the design of the UE866 interface board, the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity ε_r = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

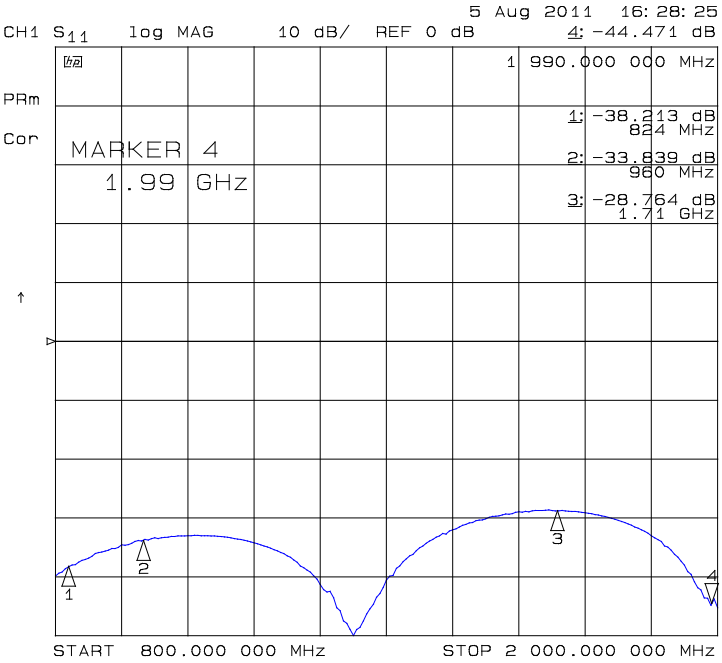
A characteristic impedance of nearly 50 Ω is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm.

Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:

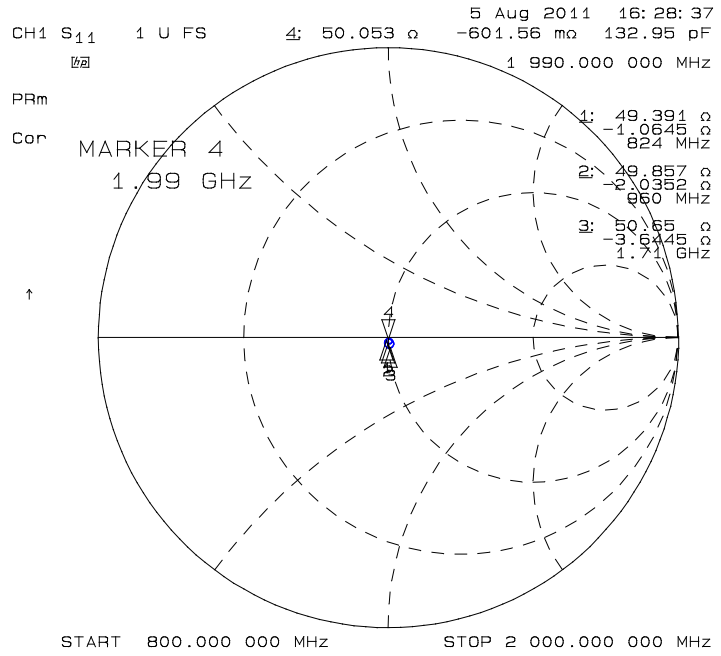


6.4.2.2 *Transmission Line Measurements*

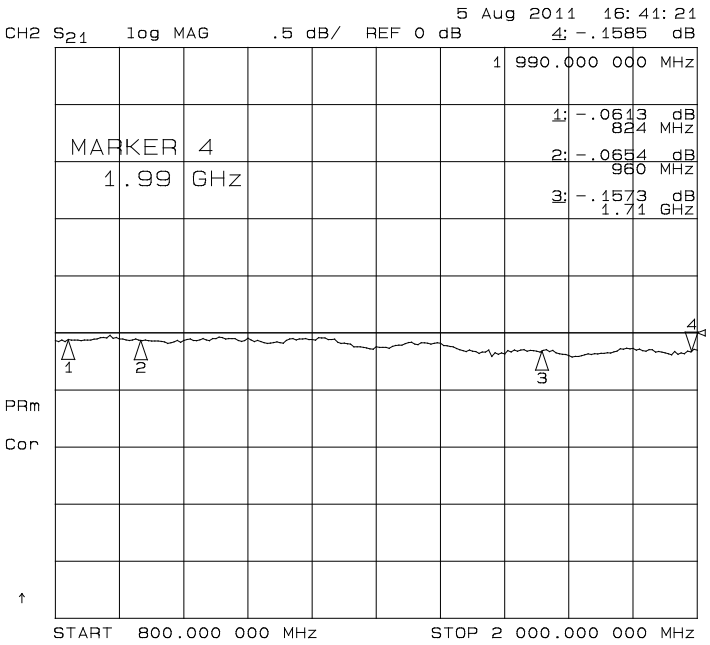
An HP8753E VNA (Full-2-port calibration) has been used in this measurement session.
A calibrated coaxial cable has been soldered at the pad corresponding to RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50 Ω load.
Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50 Ω load) is shown in the following figure:



Insertion Loss of G-CPW line plus SMA connector is shown below:



6.4.2.3 *Antenna Installation Guidelines*

Install the antenna in a place covered by the WCDMA signal.

If the device antenna is located farther than 20cm from the human body and there are no co-located transmitter then the Telit FCC/IC approvals can be re-used by the end product.

If the device antenna is located closer than 20cm from the human body or there are co-located transmitter then the additional FCC/IC testing may be required for the end product (Telit FCC/IC approvals cannot be reused).

Antenna shall not be installed inside metal cases.

Antenna shall be installed also according to antenna manufacturer instructions.

7 AUDIO SECTION

7.1 Overview

The UE866 is provided by one Digital Audio Interface.

7.2 Digital Voice Interface

The UE866 Module is provided by one DVI digital voice interface.

The Signals are available on the following Pads and alternate function of the GPIOs:

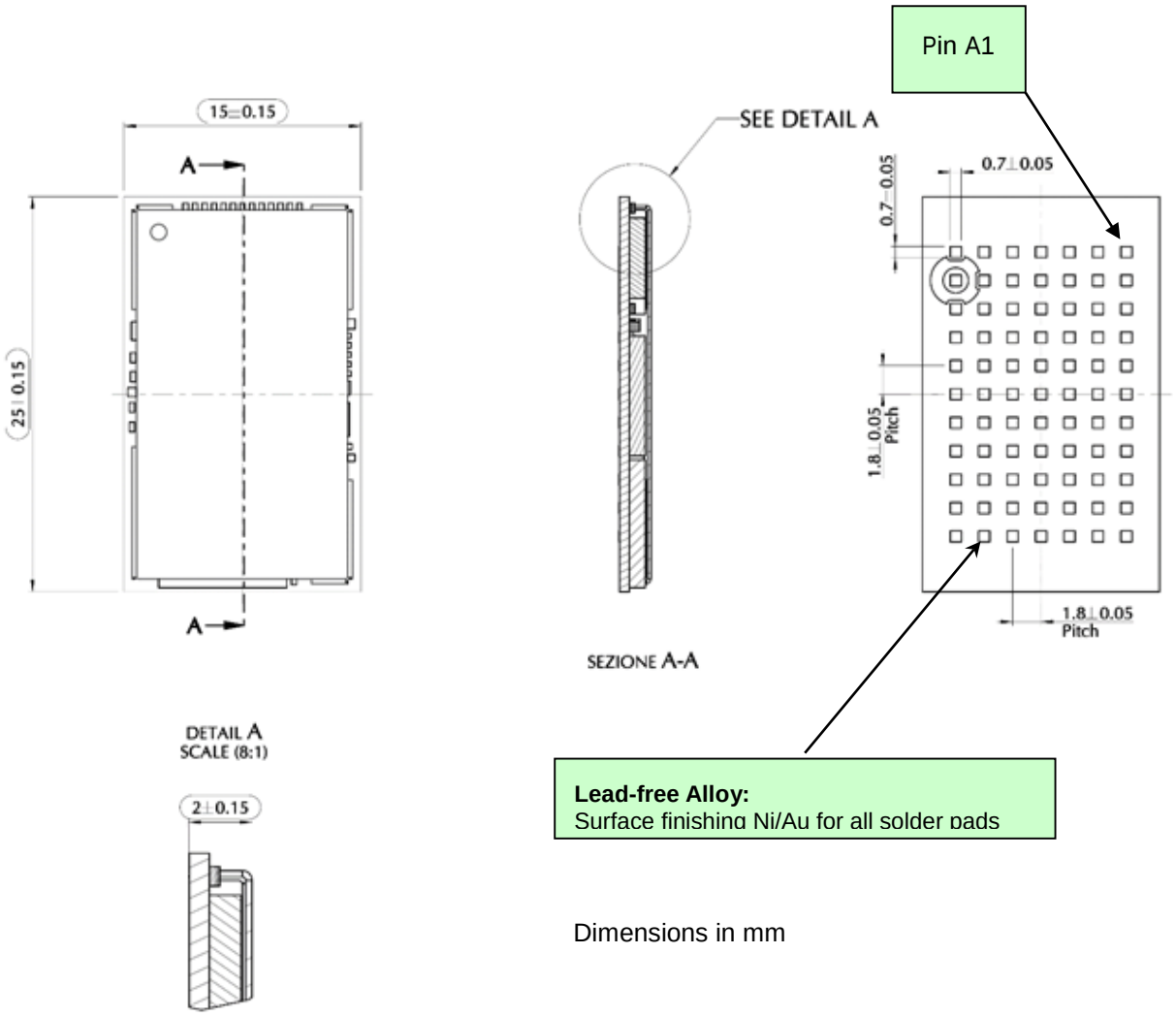
PAD	Signal	I/O	Function
C5	DVI_WA0	I/O	Digital Voice Interface (Word Alignment / LRCLK)
C6	DVI_RX	I	Digital Voice Interface (RX)
D6	DVI_TX	O	Digital Voice Interface (TX)
D5	DVI_CLK	I/O	Digital Voice Interface (BCLK)

7.2.1 CODEC Examples

Please refer to the Digital Audio Application note.

8 MECHANICAL DESIGN

8.1 Drawing



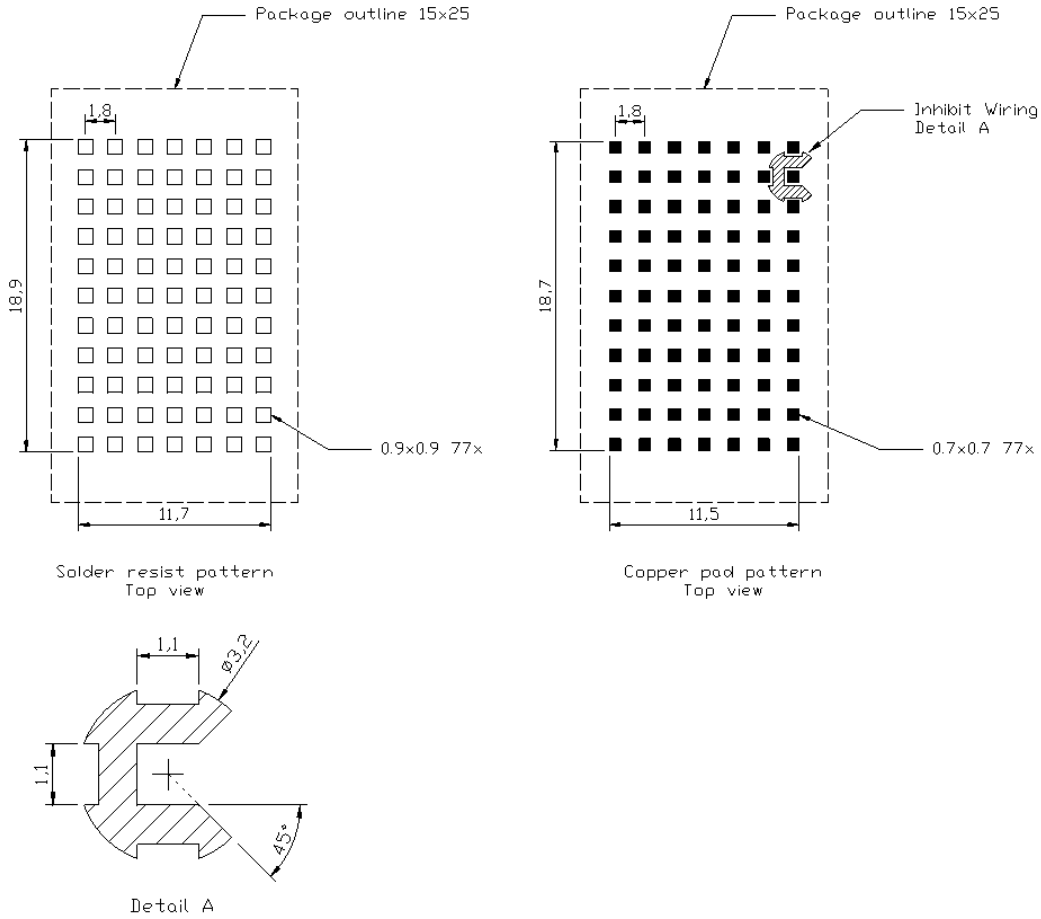
Dimensions in mm

In case of UE866-EU shield mechanical design slightly differs from UE866 other variants, but overall dimensions are the same and there is no impact on assembling and footprint area.

9 APPLICATION DESIGN

The UE866 modules have been designed in order to be compliant with a standard lead-free SMT process.

9.1 Footprint



In order to easily rework the UE866 is suggested to consider on the application a 1.5 mm placement inhibit area around the module.

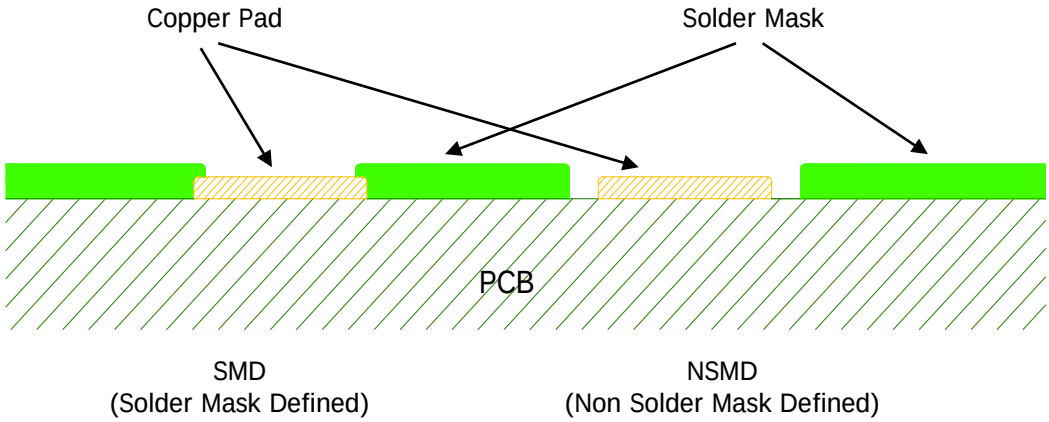
It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

NOTE:

In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

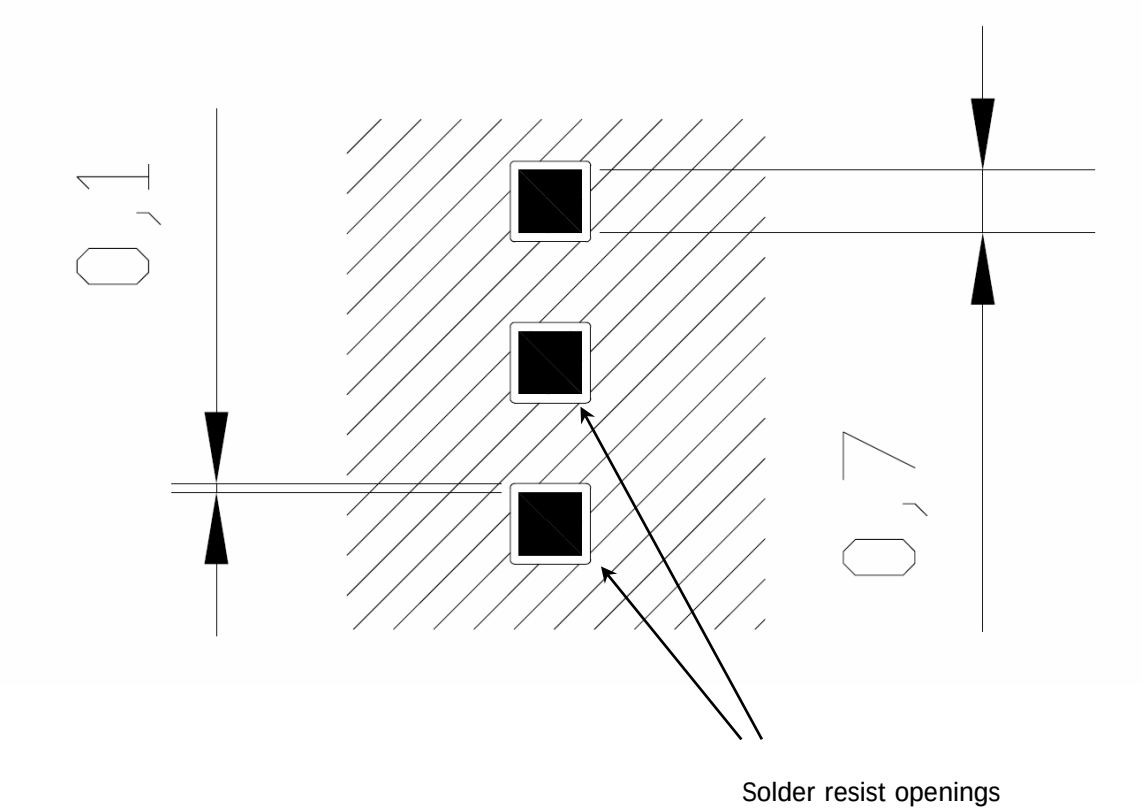
9.2 PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

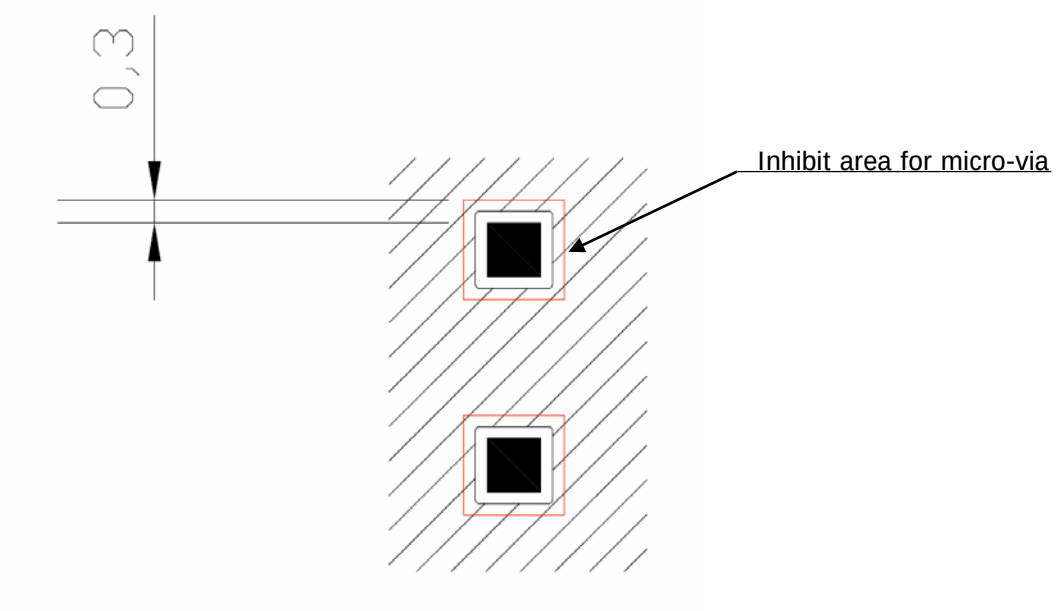


9.3 PCB pad dimensions

The recommendation for the PCB pads dimensions are described in the following image (dimensions in mm)



It is not recommended to place via or micro-via not covered by solder resist in an area of 0,3 mm around the pads unless it carries the same signal of the pad itself



Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Finish	Layer Thickness (um)	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.05 – 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.
It is not necessary to panel the application's PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

9.4 Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

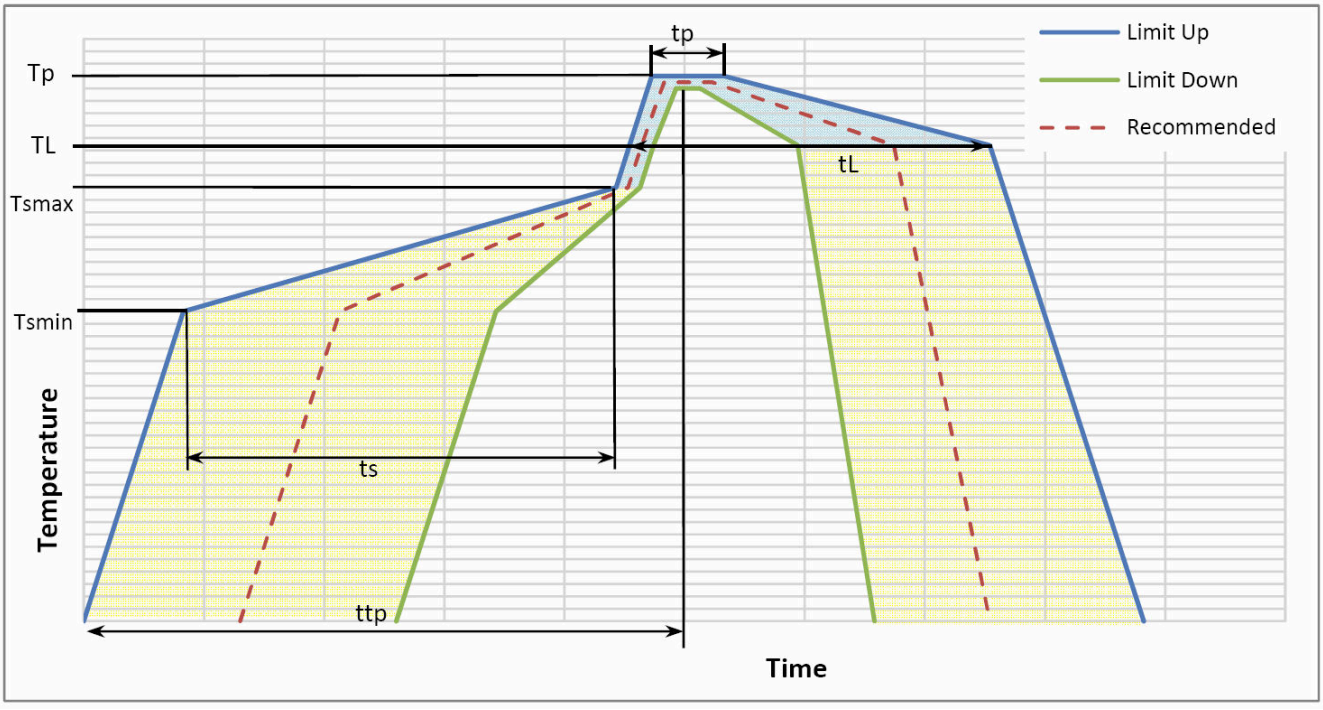
9.5 Solder paste

Item	Lead Free
Solder Paste	Sn/Ag/Cu

We recommend using only "no clean" solder paste in order to avoid the cleaning of the modules after assembly.

9.6 Solder reflow

Recommended solder reflow profile:



Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	 150°C 200°C 60-180 seconds
Tsmax to TL – Ramp-up Rate	 3°C/second max
Time maintained above: – Temperature (TL) – Time (tL)	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

NOTE:

All temperatures refer to topside of the package, measured on the package body surface

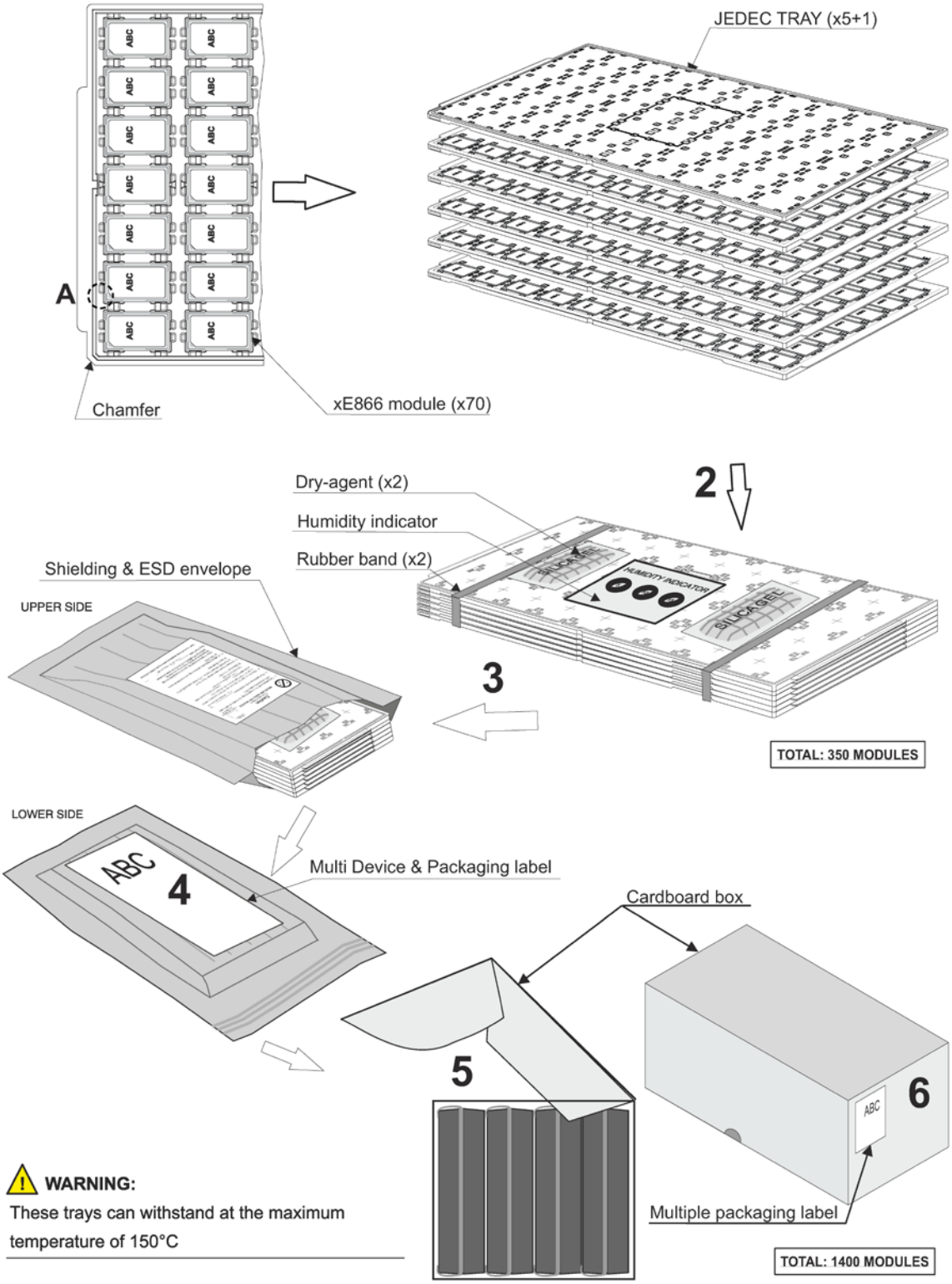
WARNING:

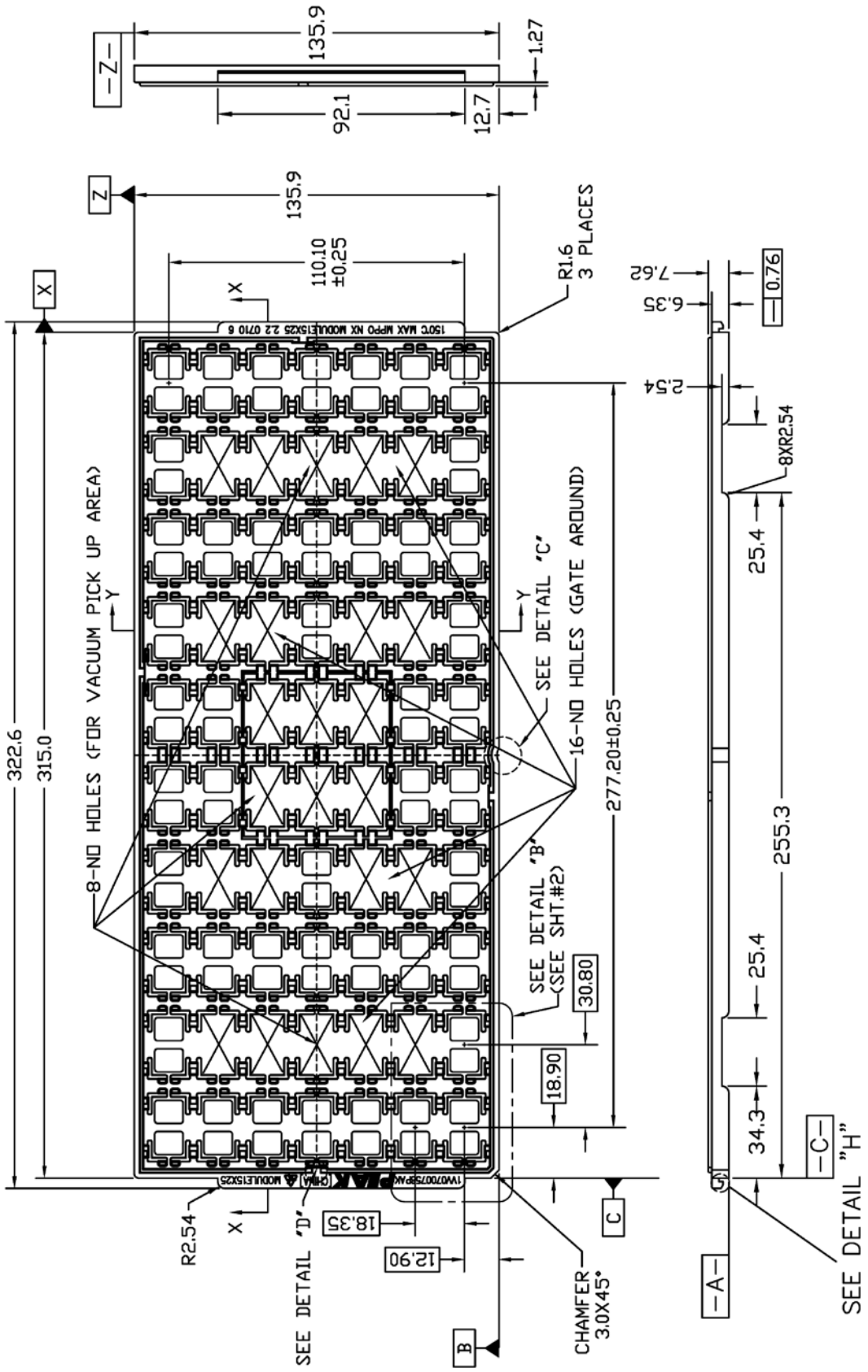
The UE866 module withstands one reflow process only.

10 PACKAGING

10.1 Tray

The UE866 modules are packaged on trays of ***70*** pieces each. These trays can be used in SMT processes for pick & place handling.





10.2 Moisture sensitivity

The UE866 is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more

11 SAFETY RECOMMANDATIONS

READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc

Where there is risk of explosion such as gasoline stations, oil refineries, etc

It is responsibility of the user to enforce the country regulation and the specific environment regulation.

The equipment is intended to be installed in restricted area locations.

Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.

Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

Maximum ambient working temperature for the standard IEC 60950-1: +60 ºC.

The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information's are available on the European Community website:

http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:

http://europa.eu.int/comm/enterprise/electr_equipment/index_en.htm

12 FCC/IC REGULATORY NOTICES

Modification statement

Telit has not approved any changes or modifications to this device by the user. Any changes or modifications could void the user's authority to operate the equipment.

Telit n'approuve aucune modification apportée à l'appareil par l'utilisateur, quelle qu'en soit la nature. Tout changement ou modification peuvent annuler le droit d'utilisation de l'appareil par l'utilisateur.

Interference statement

This device complies with Part 15 of the FCC Rules and Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Wireless notice

This equipment complies with FCC and IC radiation exposure limits set forth for an uncontrolled environment. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body. Antenna gain must be below:

Frequency Band	Gain
Band II (1900 MHz)	9.01 dBi
Band V (850 MHz)	7.76 dBd

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Cet appareil est conforme aux limites d'exposition aux rayonnements de la IC pour un environnement non contrôlé. L'antenne doit être installé de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps. Gain de l'antenne doit être ci-dessous:

Bande de fréquence	Gain
Band II (1900 MHz)	9.01 dBi
Band V (850 MHz)	7.76 dBd

L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

FCC Class B digital device notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

Reorient or relocate the receiving antenna.
Increase the separation between the equipment and receiver.
Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
Consult the dealer or an experienced radio/TV technician for help.

Wireless notice IC

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. The antenna should be installed and operated with minimum distance of 20 cm between the radiator and your body.
Antenna gain must be below:

Frequency Band	Gain
Band II (1900 MHz)	9.01 dBi
Band V (850 MHz)	4.96 dBd

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

Cet appareil est conforme aux limites d'exposition aux rayonnements de la IC pour un environnement non contrôlé. L'antenne doit être installé de façon à garder une distance minimale de 20 centimètres entre la source de rayonnements et votre corps. Gain de l'antenne doit être ci-dessous:

Bande de fréquence	Gain
Band II (1900 MHz)	9.01 dBi
Band V (850 MHz)	4.96 dBd

L'émetteur ne doit pas être colocalisé ni fonctionner conjointement avec à autre antenne ou autre émetteur.

Labelling Requirements for the Host device

The host device shall be properly labelled to identify the modules within the host device. The certification label of the module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the FCC ID and IC of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

Contains FCC ID: RI7UE866N3
Contains IC: 5131A-UE866N3

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification du module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une étiquette donnant le FCC ID et le IC du module, précédé des mots « Contient un module d'émission », du mot « Contient » ou d'une formulation similaire exprimant le même sens, comme suit :

Contains FCC ID: RI7UE866N3
Contains IC: 5131A-UE866N3

CAN ICES-3 (B) / NMB-3 (B)

This Class B digital apparatus complies with Canadian ICES-003.

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

13 DOCUMENT HISTORY

13.1 Revisions

Revision	Date	Changes
0	2014-09-19	Preliminary Version
1	2014-09-30	Updated Chapter 4.1; removed chapter 1.4
2	2014-10-03	Updated Chapter 4.1
3	2014-10-09	Updated Chapter 2, 3, 8.5
4	2015-01-08	Updated Document Template, Packaging, Flowcharts
5	2015-01-13	Added Safety Recommendations Added FCC / IC Regulatory notices Updated Chapter 2
6	2015-03-30	Updated chapters 4.2, 4.4, 4.5, 5.2, 5.8, 12 Added RX Sensitivity Added Third Party Rights
7	2015-04-17	Updated Chapter 12
8	2015-06-29	Updated Chapter 8.1
9	2015-07-17	Updated Chapter 12
10	2016-07-27	Added UE866-EU reference Updated Chapter 4, par 4.2 Updated Chapter 6
11	2016-09-21	Updated Chapter 11 Updated Chapter 4.3.1.4
12	2016-02-10	Updated Chapter 10


Design Review
120°
180°
Process
Validation
240°
RF/EMC Pre-Certification
Module Selection
60°
300°
Approvals
Support
360°
Value Added Services & Connectivity
Enterprise Integration &
Application Enablement
m2mair