WE866
HW User Guide

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TELIT
TECHNICAL
DOCUMENTATION

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APPLICABILITY TABLE

PRODUCTS

- WE866A1-P

Contents

1. INTRODUCTION

1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit WE866 module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their apllications using our WE866 modules.

1.3. Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

- TS-EMEA@telit.com
- TS-AMERICAS@telit.com
- TS-APAC@telit.com
- TS-SRD@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.5. Related Documents

2. OVERVIEW

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit WE866 module. In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit WE866 module. For further hardware details that may not be explained in this document refer to the Telit WE866 Product Description document where all the hardware information is reported.

NOTE:

(EN) The integration of theWE866 cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare WE866 all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des WE866 Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija WE866 modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo WE866 debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire WE866 dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי WE866 עם המוצר.

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3. PINS ALLOCATION

3.1. Pin-out

Pin	Signal	I/O	Function	Type	Comment
Asynchronous Serial Port (USIF0) - Prog. / Data + HW Flow Control					
A4	TXD	I	Serial data input from DTE		
A5	RXD	O	Serial data output to DTE		
A1	RTS	I	Input for Request to send signal (RTS) from DTE		
B1	CTS	O	Output for Clear to Send signal (CTS) to DTE		
Serial Peripheral Interface (SPI)					
A3	SPI_MISO	O	Module data output Host (Master) data input		
B2	SPI_MOSI	I	Module data input Host (Master) data output		
A2	SPI_CLK	I	SPI clock from Host to module		
B3	SPI_CSN	I	SPI Chip Select (active low)		Active low
Miscellaneous Functions					
D3	HIB*	I	Hibernate signal input to the module (active low)		Active low
B4	HOST_INTR	O	Interrupt output (active high)		
G4	RESET*	I	Reset input for the device (active low)		Active low

G5	ON_OFF	I	Input command for power ON	
G6	VDD	O	Supply output for external accessories	
G2	ANT	I/O	WiFi Antenna	RF
Power Supply				
E1	VBATT	-	Main Power supply	Power
E2	VBATT	-	Main Power supply	Power
C3	GND	-	Ground	Power
D1	GND	-	Ground	Power
D2	GND	-	Ground	Power
E3	GND	-	Ground	Power
F1	GND	-	Ground	Power
F2	GND	-	Ground	Power
F3	GND	-	Ground	Power
G1	GND	-	Ground	Power
G3	GND	-	Ground	Power
F6	GND	-	Ground	Power
Reserved				
C1	RESERVED		RESERVED	
C2	RESERVED		RESERVED	
D3	RESERVED		RESERVED	

C4	RESERVED	RESERVED
D4	RESERVED	RESERVED
E4	RESERVED	RESERVED
F4	RESERVED	RESERVED
B5	RESERVED	RESERVED
C5	RESERVED	RESERVED
D5	RESERVED	RESERVED
E5	RESERVED	RESERVED
F5	RESERVED	RESERVED
A6	RESERVED	RESERVED
B6	RESERVED	RESERVED
C6	RESERVED	RESERVED
D6	RESERVED	RESERVED
E6	RESERVED	RESERVED
A7	RESERVED	RESERVED
B7	RESERVED	RESERVED
C7	RESERVED	RESERVED
D7	RESERVED	RESERVED
E7	RESERVED	RESERVED
F7	RESERVED	RESERVED

G7	RESERVED	RESERVED

Warning – Reserved pins must not be connected.

Warning – VDD output must not be used to supply any device on the customer application.

It is only provided as reference/supply voltage when voltage translation to 1V8 CMOS is needed.

When its use is necessary, it is strongly recommended to connect VAUX through a series resistor as closed as possible to the module in order to reduce the inrush current of the internal DC/DC supply. Use a low value resistor (e.g. 10 ohm, 1/3W) with a maximum power rating to drained current.

3.2. LGA Pads Layout

TOP VIEW

	A	B	C	D	E	F	G
1	RTS	CTS	RES	GND	VBATT	GND	GND
2	SPI_CLK	SPI_MOSI	RES	GND	VBATT	GND	ANT
3	SPI_MISO	SPI_CS	GND	nHIB	GND	GND	GND
4	TXD	HOST_INTR	RES	RES	RES	RES	RESET*
5	RXD	RES	RES	RES	RES	RES	ON_OFF
6	RES	RES	RES	RES	RES	GND	VDD
7	RES	RES	RES	RES	RES	RES	RES

4. POWER SUPPLY

4.1. Power Supply Requirements

The external power supply must be connected to VBATT signals and must fulfill the following requirements:

Power Supply	
Nominal Supply Voltage	3.8 V
Normal Operating Voltage Range	3.1 V÷ 4.50 V

The Operating Voltage Range MUST never be exceeded; care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.

If the voltage drop is exceeding the limits it could cause a Power Off of the module.

Please note that the operating voltage limits MUST never be exceed, including voltage overshoots and drops.

4.2. Power Consumption

The WE866 expected power consumption is reported on the table below. All values are at 25°C and VBATT=3.8V, if not otherwise stated.

Functional mode		Current consumption(*) (typ) [mA]
Transmission at maximum power level	802.11b, 1Mbps	285
	802.11g, 6Mbps	261
	802.11g, 54Mbps	236
Reception	802.11b, 1Mbps	66
	802.11g, 54Mbps	66
Idle connected		14
Peak calibration		<400
Hibernate		0.03

(*) preliminary values

4.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- The electrical design
- The thermal design
- Thermal PCB layout

4.3.1. Electrical Design Guidelines

The electrical design of the power supply depends strongly on the power source from which this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

4.3.1.1. +5V Source Power Supply Design Guidelines

- Because of the small difference between the input and output voltage, a switching converter is not the best choice, therefore a low-dropout regulator is required.
- When using a linear regulator, a proper heat sink must be provided in order to dissipate the power generated.
- A low-ESR, bypass capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the WE866, a 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode should be inserted close to the power input, in order to save the WE866 from power polarity inversion.

4.3.1.2. +12V Source Power Supply Design Guidelines

- In this case, better efficiency of switching regulators can be exploited to generate the required 3.8V
- Switching frequencies of 500kHz or above are preferable, because of the smaller inductor size and the faster transient response.
- For car Pb battery, the input voltage can rise up to 15.8V and this should be kept in mind when choosing components: all components in the power supply must withstand this voltage. A spike protection diode has to be inserted close to the power input.
- A low-ESR, bypass capacitor of adequate capacity must be provided in order to cut current absorption peaks. 100µF, 10V is usually enough.
- A protection diode should be inserted close to the power input, to avoid damage to the WE866 from polarity inversion. This can be the same diode used for spike protection.

4.3.1.3. Battery Source Power Supply Design Guidelines

- A single 3.7V Li-Ion cell battery can be used to power the WE866 module.
- A low-ESR, bypass capacitor of adequate capacity must be provided in order to cut current absorption peaks. 100µF, 10V is usually enough.
- The WE866 module must be protected from polarity inversion: this can be done with a protection diode, or by exploiting a suitable battery connector

Both three-cell Ni/Cd or Ni/MH 3.6V batteries, and 4V Pb batteries, can feature maximum voltages above the maximum allowed VBATT for the WE866, which is 4.5V. For this reason, they must not be directly connected to the module. Only Li-Ion types are recommended for direct connection.

4.3.2. Power Supply PCB layout Guidelines

As seen on the electrical design guidelines, the power supply shall have a low-ESR capacitor on its output, to cut the current peaks, and a protection diode on its input, to protect the VBATT pins from polarity inversion. The placement of these components is crucial to ensure the correct working of the circuitry. A misplaced component can be useless, or even detrimental to the power supply performances.

- The low-ESR, bypass capacitor must be placed close to the WE866 VBATT pads, or close to the inductor if a switching regulator is used.
- The protection diode must be placed close to the input power connector.
- The pcb power traces must be wide enough to ensure negligible voltage drop even at the highest rated current consumption for the WE866.
- Use of a good, common ground plane is recommended.

4.4. VDD Power Output

A regulated 1.85V supply voltage is provided on pin G6 of the WE866 module. Please note that this voltage has the sole purpose to be a reference, e.g. for external voltage translators. No external devices must be powered from this voltage.

5. DIGITAL SECTION

5.1. Logic Levels

The following table shows the logic level specifications use in WE866:

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8V) when on	-0.3V	+2.1V

Level	Min	Max
V_{IH} Input high level	1.5V	2.1V
V_{IL} Input low level	0V	0.4V
V_{OH} Output high level	1.6V	2.1V
V_{OL} Output low level	0V	0.2V
V_{IL} nRESET	0V	0.6V

The nRESET pin must be held below 0.6V for the device to register a reset.

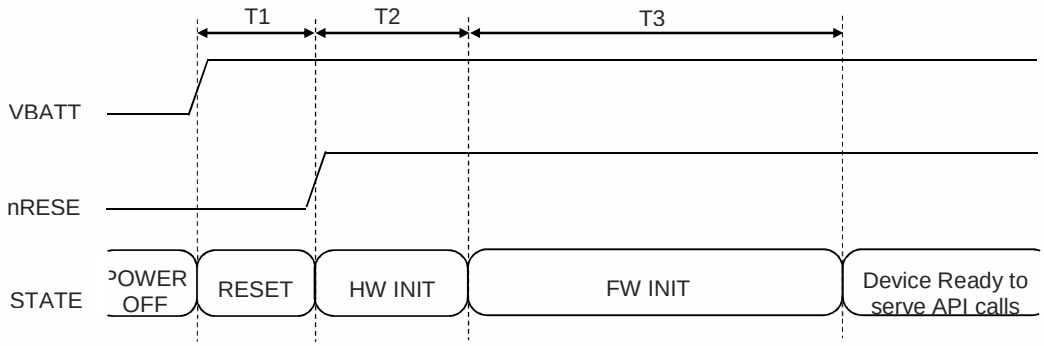
Level	Typical
Input current	5nA
Output current	6mA

5.2. Power On

The module is usually in state on mode. ON_OFF line is internally pulled up and when VBATT is applied the module is automatically turned on.

The device need 3 ms to switch on the device and have all the internally voltage stable, this soft start prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. nRESET must be held low until the VBATT supply to the device is driven and stable.

In order to switch on the device it must be applied a input logic high level to ON_OFF pin.



ITEM	NAME	DESCRIPTION	TYPICAL
T1	Supply settling time		3ms
T2	Hardware wake-up		25ms
T3	Initialization time	Internal XTAL stabilization plus firmware initialization time plus radio calibration	1.35s

Tip or Information – Don't use any pull up resistor on the ON_OFF line, it is internally pulled up.

5.3. Power Off

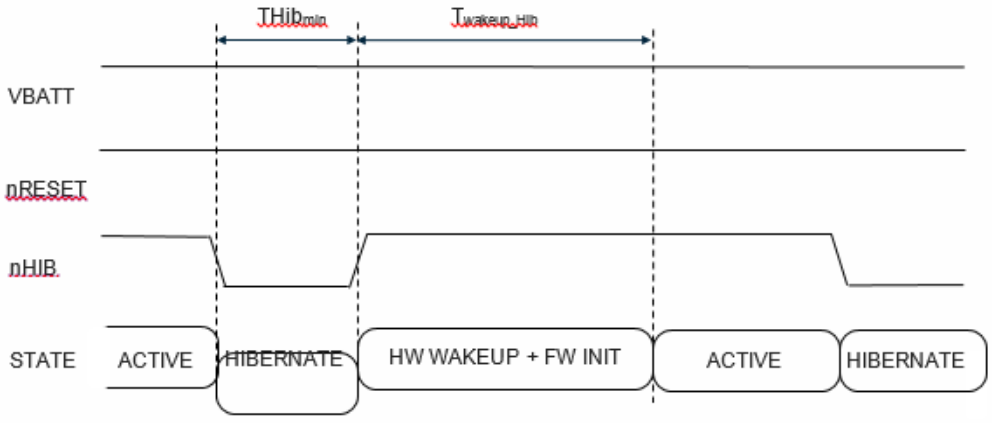
In order to switch off the device it's necessary to force the ON_OFF pin to 0V.

5.4. Low power deep sleep

The low power deep sleep (LPDS) mode is an energy-efficient and transparent sleep mode that is entered automatically during periods of inactivity based on internal power optimization algorithms. The device can wake up in less than 3ms from the internal timer or from any incoming host command. Typical battery drain in this mode is 115µA. During LPDS mode, the device retains the software state and certain configuration information. The operation is transparent to the external host; thus, no additional handshake is required to enter or exit this sleep mode.

5.5. Hibernate

The hibernate mode is the lowest power mode in which all of digital logic is power-gated. Only a small section of the logic powered directly by the main input supply is retained. The RTC is kept running and the device wakes up once the nHIB line is asserted by the host device. Ultralow leakage when disabled (hibernate mode) with a current of less than 4 µA with the RTC running. The average wake-up time is longer than LPDS mode, is about 50ms.



HIBERNATE timing diagram

ITEM	NAME	DESCRIPTION	MIN	TYP	MAX
$THib_{min}$	Minumum hibernate time	Minimum pulse width of nHIB being low	10ms		
T_{wakeup_Hib}	Hardware wakeup time plus firmware initialization time	(1)		50ms	

(1) If temperature changes by more than 20°C, initialization time from HIB can increase by 200ms due to radio calibration.

5.6. Shutdown

The shutdown mode is the lowest power-mode system-wise. All device logics are off, including the real.time clock (RTC). The wake-up time in this mode is longer than hibernate, is about 1.1s.

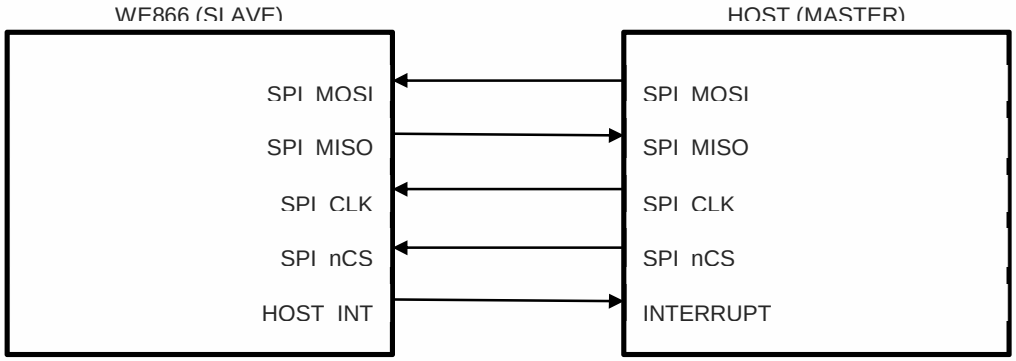
State	Wake-up Time	Average Power Consumption
Low Power Deep Sleep (LPDS)	3ms	115µA
Hibernate	50ms	4µA
Shutdown	1.1s	1µA

5.7. Communication ports

5.7.1. SPI

Module WE866 is considered as a slave when it is interfaced with a Host which acts as master. In addition to the standard SPI lines (MOSI, MISO, CLK, CS) it can be used also HOST_INT line. WE866 can interrupt the host using HOST_INT line to initiate the data transfer over the interface. The SPI interface can work up to a speed of 20MHz.

PAD	Signal	I/O	Function
B2	SPI_MOSI	I	Module data input, Host data output
A3	SPI_MISO	O	Module data output, Host data input
A2	SPI_CLK	I	SPI clock from Host to module
B3	SPI_nCS	I	SPI Chip select (active low) from Host
B4	HOST_INT	O	Interrupt from Module to Host (Optional)



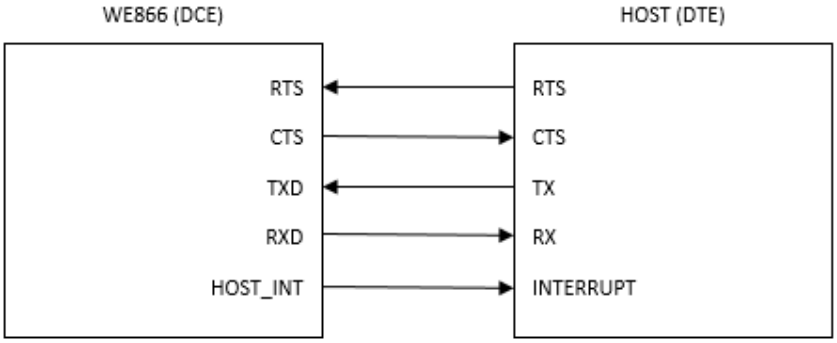
5.7.2. UART

In the table below are listed the UART configuration of WE866.

PROPERTY	WE866 CONFIGURATION
Baud rate	115200 bps, no auto-baud rate detection, can be changed by the host up to 3 Mbps using a special command
Data bits	8 bits
Flow control	CTS/RTS
Parity	None
Stop bits	1
Bit order	LSBit first
Host interrupt polarity	Active high
Host interrupt mode	Rising edge or level 1
Endianness	Little-endian only, WE866 does not support automatic detection of the host length while using the UART interface

PAD	Signal	I/O	Function
A1	RTS	I	Input for Request to send signal (RTS) from DTE
B1	CTS	O	Output for Clear to send signal (CTS) to DTE
A4	TXD	I	Serial data input (TXD) from DTE
A5	RXD	O	Serial data output (RXD) to DTE
B4	HOST_INT	O	Interrupt from Module to Host (Optional)

Figure.. shows the typical UART topology comprised of four standard UART lines (RTS, CTS, TX and RX) plus an optional line INTERRUPT from WE866 module to the host controller to allow efficient low-power mode. The configuration with INTERRUPT line offers the maximum communication reliability and flexibility between the host and the module.



6. RF SECTION

6.1. Bands Variants

The WE866 module operates in the 2.400-2.500 GHz ISM band, and it complies with protocols 802.11b/g/n. Supported channels are 1-13, at frequencies listed in the following table:

Channel	Frequency [MHz]
1	2412
2	2417
3	2422
4	2427
5	2432
6	2437
7	2442
8	2447
9	2452
10	2457
11	2462
12	2467
13	2472

Please note that channel availability may vary according to regional regulations.

6.2. TX Output power

All measures have been taken at VBATT = 3.8V, Tamb = 25°C, if not otherwise stated.

Protocol	Datarate [Mbps]	Maximum RMS output power (typ.) (*) [dBm]
802.11b	1	17
	2	17
	11	17.25
802.11g	6	16.25
	9	16.25
	54	13.5
802.11n	MCS7	12.0

(*) preliminary values

Please note that maximum allowed output power may depend on regional regulations.

6.3. RX Sensitivity

All measures have been taken at VBATT = 3.8V, Tamb = 25°C, if not otherwise stated.

Protocol	Datarate [Mbps]	Sensitivity (typ.)(*) [dBm]
802.11b (PER < 8%)	1	-94.7
	2	-92.6
	11	-87.0
802.11g (PER < 10%)	6	-89.0
	9	-88.0
	54	-73.0
802.11n (PER < 10%)[1]	MCS0	-88.0
	MCS7	-70.0
	MCS7 (mixed mode)	-69.0

(*) preliminary values

6.4. Antenna requirements

Special care must be taken during the design of the RF section on the application board.

RF performance degradation, and infringements of emission limits, may arise if the following recommendations are not respected.

A 50Ω antenna is required. Telit's WE866 interface features an SMA connector for an external antenna, but other choices are possible, such as a chip or a printed one. In case an integrated or printed antenna is used, it is recommended to place it on the edge of the application board.

Since it may be necessary to tune the antenna impedance to 50Ω, it is recommended to foresee a PI matching network between the WE866 and the antenna, at least during first prototyping: if not required, a series 0Ω-resistor can be used, leaving the two shunt components unpopulated.

In order to be able to reuse Telit's FCC certification, the antenna on the application board shall have a gain equal to the one recommended by Telit, or lower.

6.4.1. PCB Design guidelines

The WE866 module provides a 50Ω antenna pad, which has to be routed to the antenna connector (or the integrated antenna) by means of a transmission line.

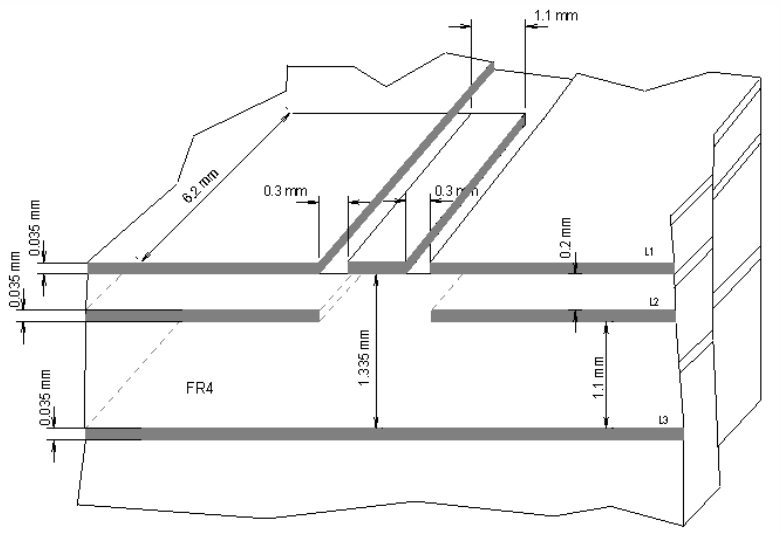
It is vital that the impedance of this line is controlled to 50Ω. The line should be as short as possible, and keep a constant cross section, without abrupt curves. It shall be isolated from any other noise source: in particular, trace shall not be crossed by other lines in adjacent layers. Instead, a continuous ground plane is recommended under the antenna trace, and a ground via curtain should connect it to the coplanar ground planes.

As an example of a possible implementation, the details of the antenna trace on the WE866 interface board are described in this section.

A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity εr = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.

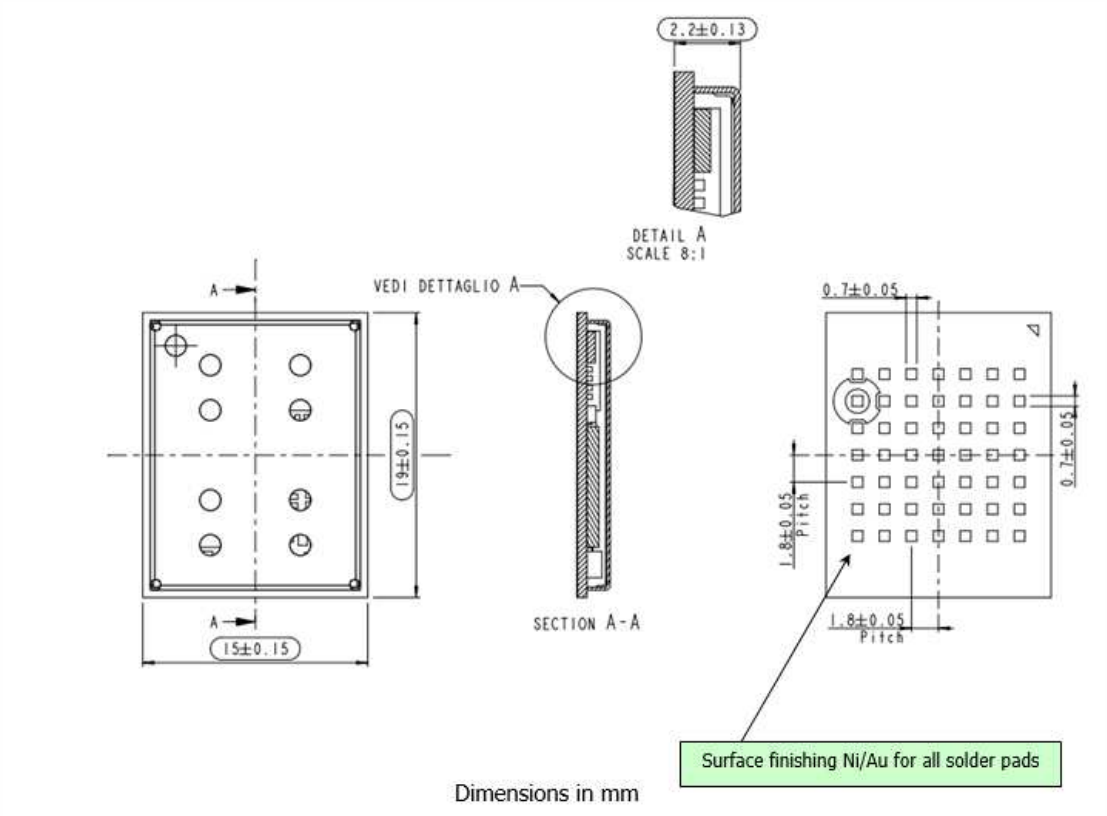
A characteristic impedance of nearly 50 Ω is achieved using trace width of 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:



6.4.2. PCB Guidelines in case of FCC Certification

7. MECHANICAL DESIGN

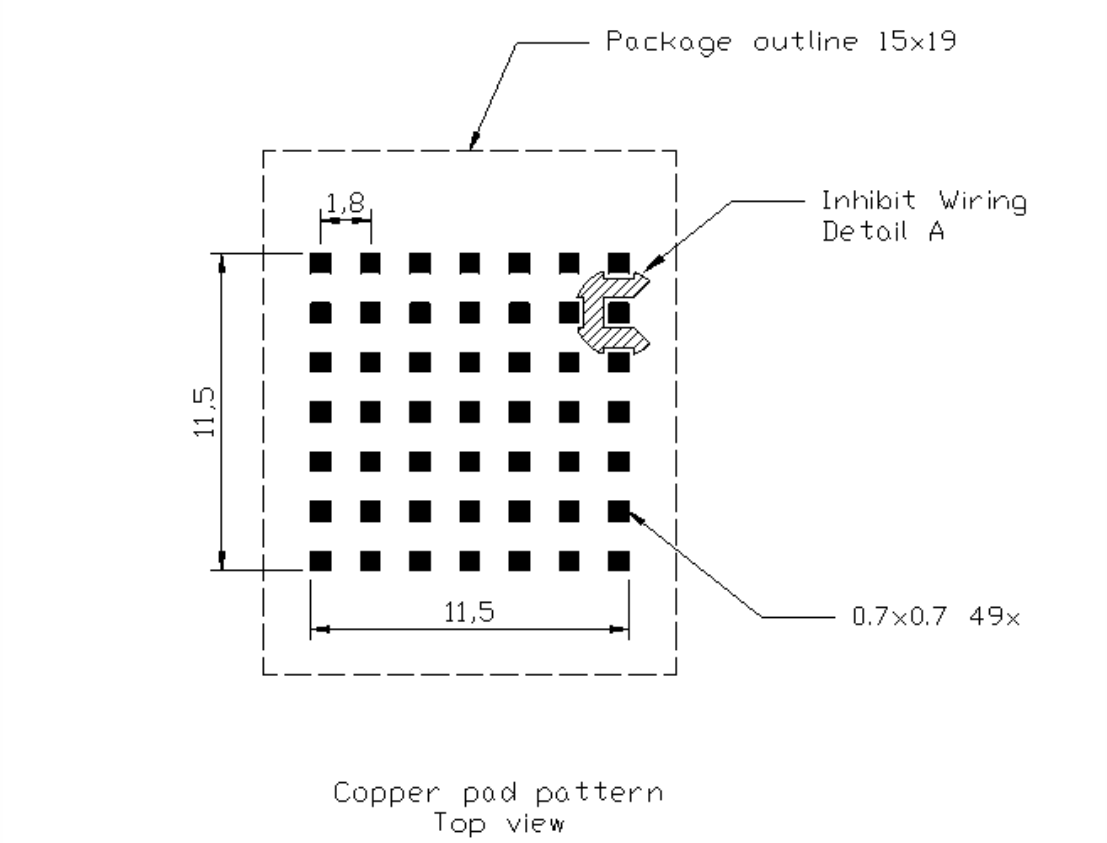
7.1. Drawing



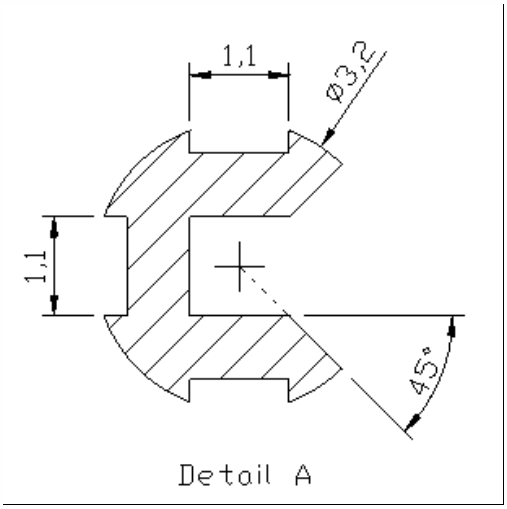
8. APPLICATION PCB DESIGN

8.1. Footprint

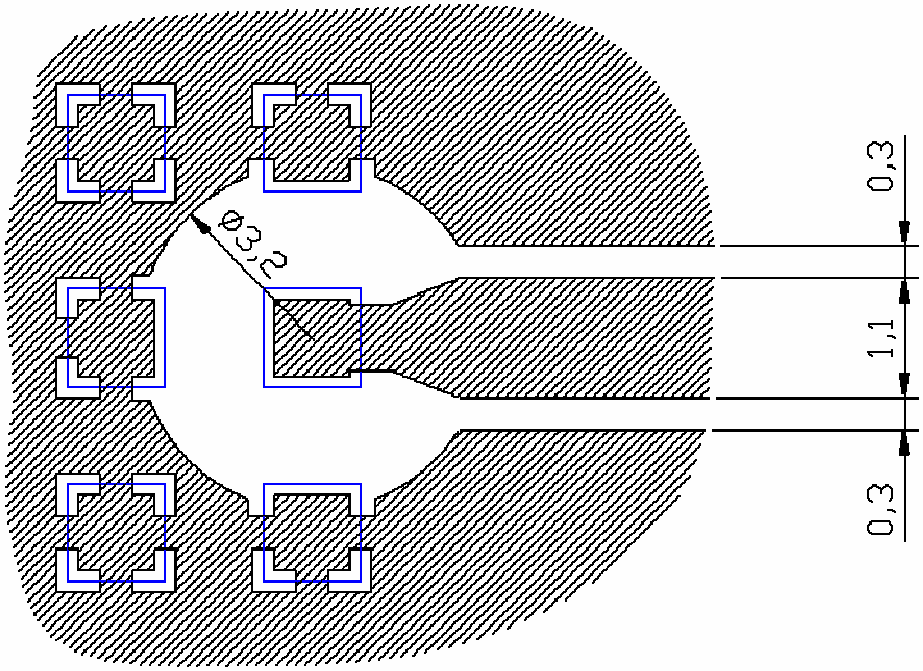
Recommended footprint for the application:

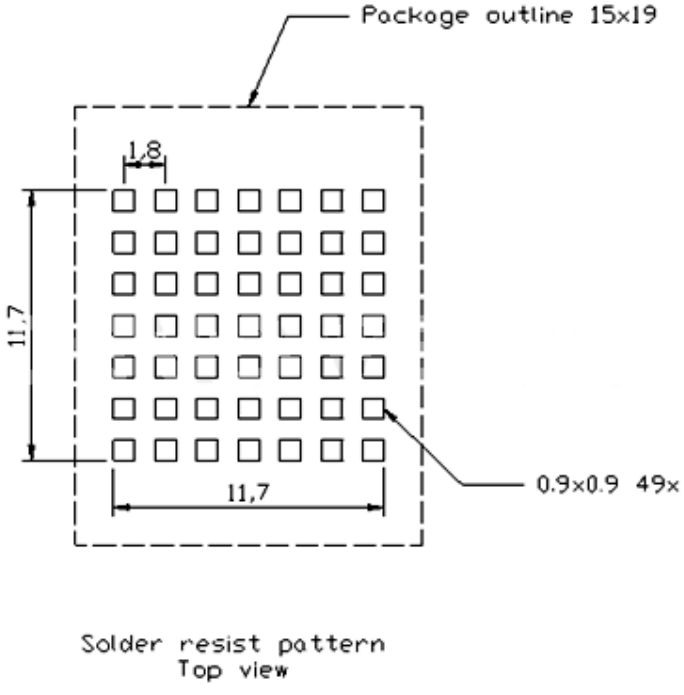


Copper pad pattern
Top view



Detail A





Solder resist pattern
Top view

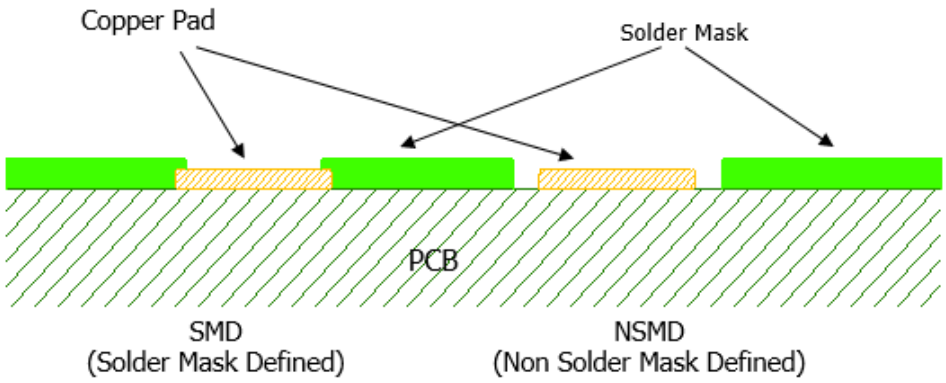
In order to easily rework the WE866 is suggested to consider on the application a 1.5 mm placement inhibit area around the module.

It is also suggested, as common rule for an SMT component, to avoid having a mechanical parts of the application in direct contact with the module.

Tip or Information – In the customer application, the region under WIRING INHIBIT (see figure above) must be clear from signal or ground paths.

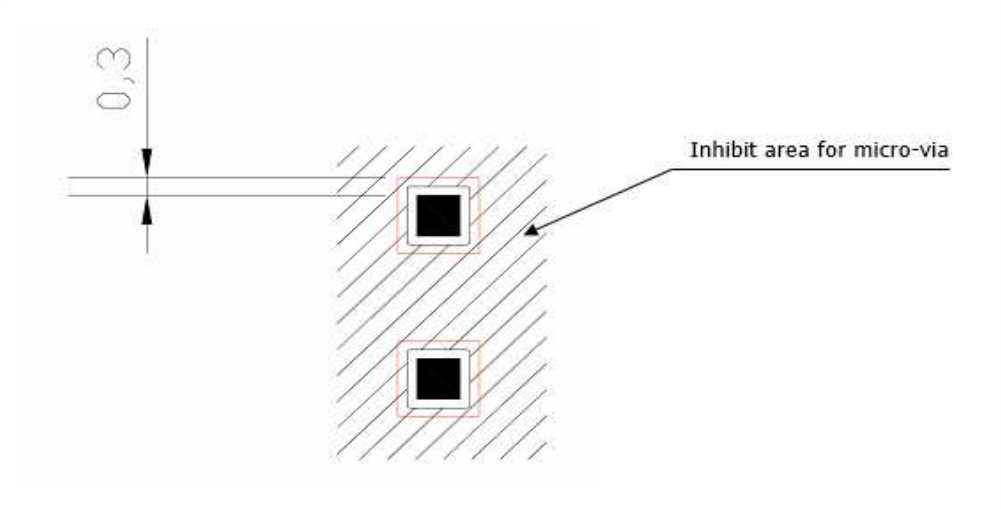
8.2. PCB pad design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



8.3. PCB pad dimensions

It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see following figure).



Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Finish	Layer thickness [µm]	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.03 – 0.15	Good solderability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

8.4. Stencil

Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120 µm.

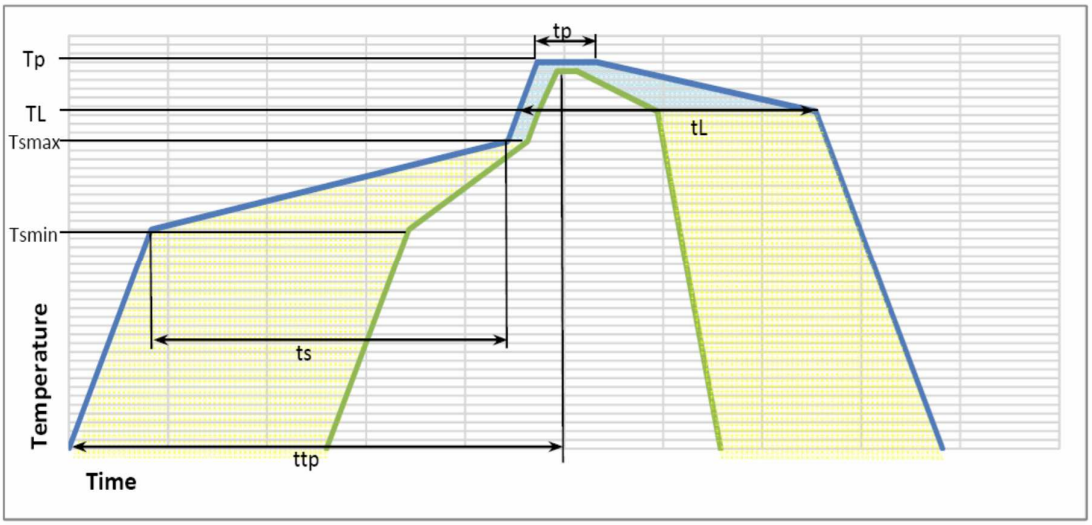
8.5. Solder paste

	Lead free
Solder paste	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

8.6. Solder Reflow

Recommended solder reflow profile



Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max
Preheat **– Temperature Min (Tsmin)** **– Temperature Max (Tsmax)** **– Time (min to max) (ts)**	 150°C 200°C 60-180 seconds
Tsmax to TL **– Ramp-up Rate**	 3°C/second max
Time maintained above:	

– Temperature (TL) **– Time (tL)**	217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature	8 minutes max.

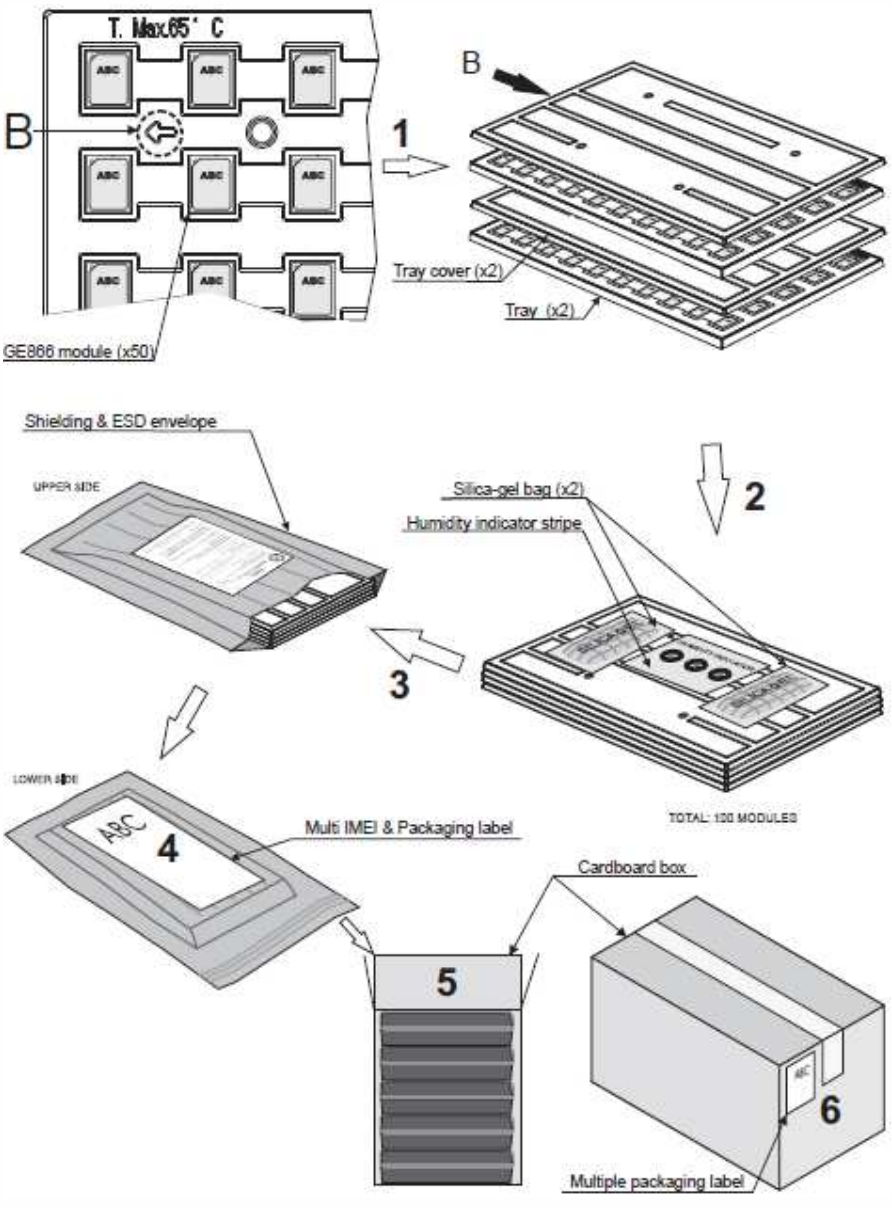
Tip or Information – All temperatures refer to topside of the package, measured on the package body surface.

Caution or Warning –WE866 module withstands one reflow process only.

9. PACKAGING

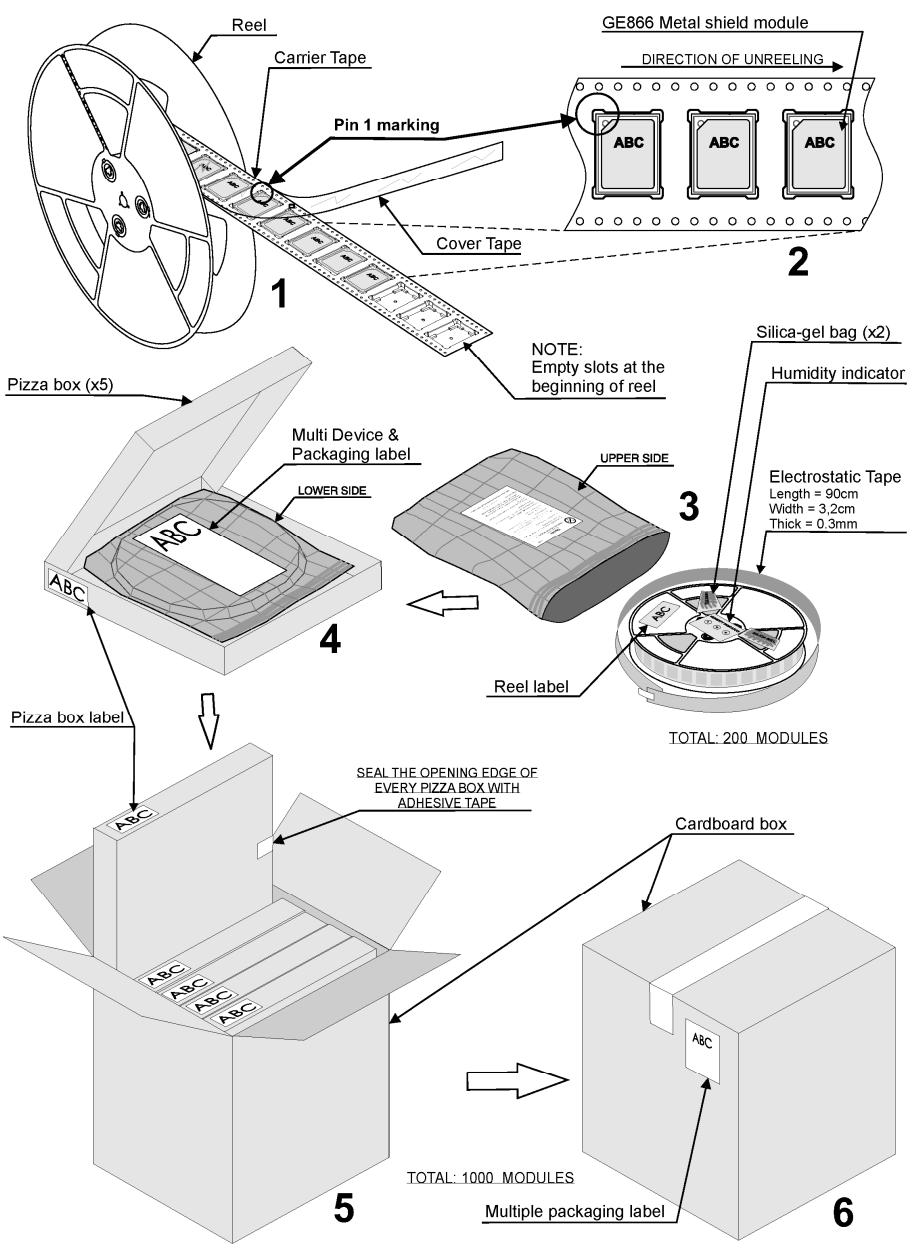
9.1. Tray

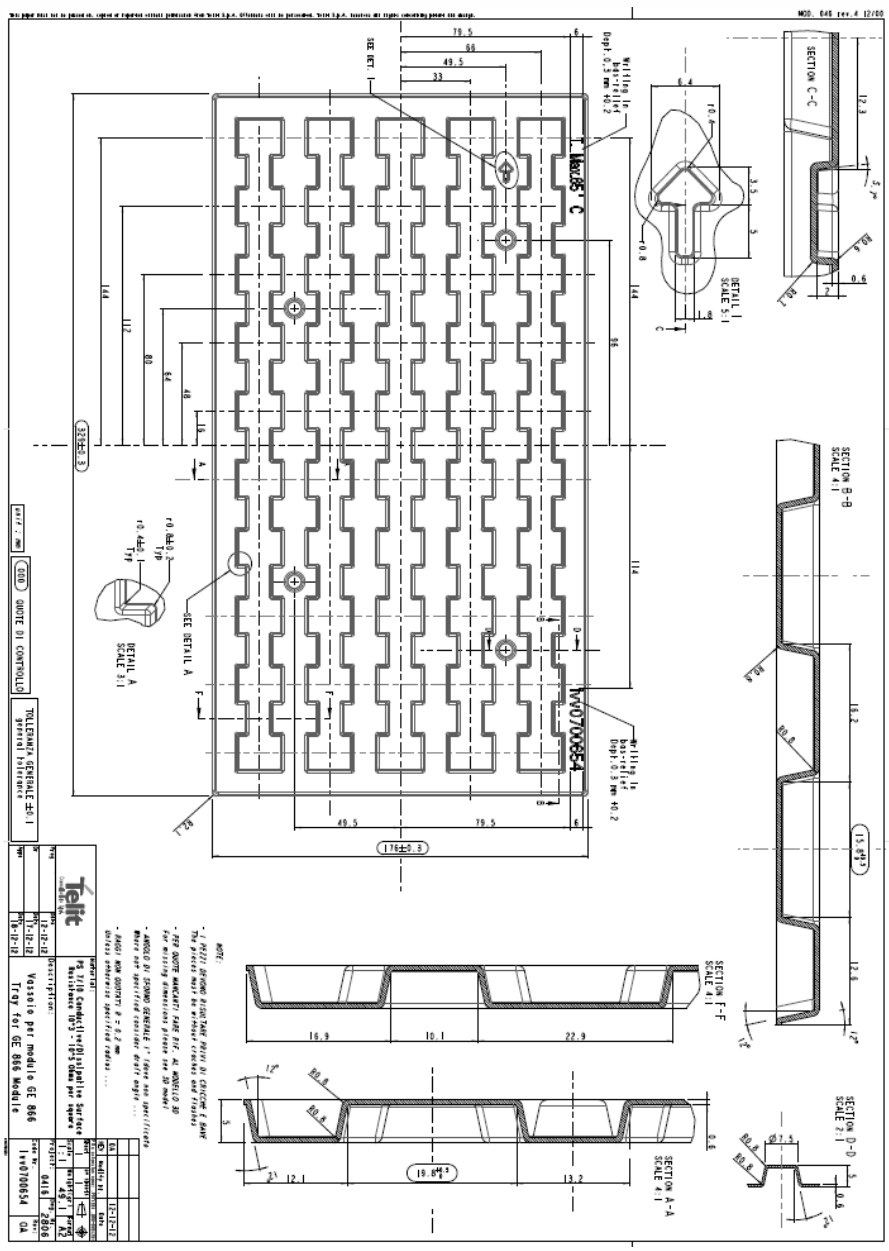
The WE866 modules are packaged on trays of 50 pieces each when small quantities are required (i.e. for test and evaluation purposes). Trays are not designed to be used in SMT processes for pick and place handling.



9.2. Reel

The WE866 modules are packaged on reels of 200 pieces each, see picture below.





Caution or Warning –These trays can withstand at the maximum temperature of 65°C.

9.3. Moisture sensitivity

The moisture sensitivity level of the Product is “3” according with standard IPC/JEDEC J-STD-020, take care of all the relative requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) The shelf life of the Product inside of the dry bag is 12 months from the bag seal date, when stored in a non-condensing atmospheric environment of < 40°C and < 90% RH.

b) Environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033B.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033B paragraph 5.2” is respected.

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more.

10. CONFORMITY ASSESSMENT ISSUES

10.1. FCC/IC Regulatory notices

11. SAFETY RECOMMENDATIONS

11.1. READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country regulation and the specific environment regulation.

Do not disassemble the product; any mark of tampering will compromise the warranty validity. We recommend following the instructions of the hardware user guides for correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conformed to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation.

The European Community provides some Directives for the electronic equipment introduced on the market. All of the relevant information is available on the European Community website:

http://ec.europa.eu/enterprise/sectors/rtte/documents/

The text of the Directive 99/05 regarding telecommunication equipment is available,

while the applicable Directives (Low Voltage and EMC) are available at:

http://ec.europa.eu/enterprise/sectors/electrical/

12. ACRONYMS

TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
HS	High Speed
DTE	Data Terminal Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
UART	Universal Asynchronous Receiver Transmitter
HSIC	High Speed Inter Chip
SIM	Subscriber Identification Module
SPI	Serial Peripheral Interface
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
MOSI	Master Output – Slave Input
MISO	Master Input – Slave Output
CLK	Clock
MRDY	Master Ready

SRDY	Slave Ready
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer

13. DOCUMENT HISTORY

Revision	Date	Changes
0	2016-10-27	First issue
1	2016-12-06	Updated Pin Out Table

SUPPORT INQUIRIES

Link to **www.telit.com** and contact our technical support team for any questions related to technical issues.

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