CE910-SL Hardware User Guide

1VV0301187 Rev.3 – 2016-5-04

Making machines talk.

APPLICABILITY TABLE

PRODUCT
CE910-SL

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

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Contents

1. Introduction

1.1. Scope

The aim of this document is the description of typical hardware solutions useful for developing a product with the Telit CE910-SL module.

1.2. Audience

This document is intended for Telit customers who are about to implement their applications using our CE910-SL modules.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where to buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Please keep us informed of comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "General Product Description" gives an overview of the features of the product.

Chapter 3: "CE910-SL Module Connections" deals with the pin out configuration and layout.

Chapter 4: "Hardware Commands" How to operate the module via hardware.

Chapter 5: "Power supply" Power supply requirements and general design rules.

Chapter 6: "Antenna" The antenna connection and board layout design are the most important parts in the full product design.

Chapter 7: "USB Port" The USB port on the Telit CE910-SL is the core of the interface between the module and OEM hardware.

Chapter 8: "Serial port" Refers to the serial port of the Telit CE910-SL.

Chapter 9: "Audio Section overview" Refers to the audio blocks of the Base Band Chip of the CE910-SL Telit Module.

Chapter 10: "General Purpose I/O" How the general purpose I/O pads can be configured.

Chapter 11: "ADC section" Deals with this one kind of converter.

Chapter 12: "Test Point" Deals with Test Point.

Chapter 13: "Mounting CE910-SL on the Application" Mechanical dimensions and recommendations on how to mount the module on the user's board.

Chapter 14: "Packing System" Deals with packing system.

Chapter 15: "Application Design Guide" Deals with the design of host system for download or upgrade.

Chapter 16: "Safety Recommendation" provides some safety recommendations that must be followed by the customer in the design of the application that makes use of the Telit CE910-SL.

Chapter 17: "Document History" provides document revision history of the Telit CE910-SL.

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module. If these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- CE910-SL Software User Guide, 1VV0301186
- CE910-SL AT Commands Reference Guide, 80462ST10669A
- Telit xE910 Global Form Factor Application Note, 80000NT10060A
- Telit xE910 RTC Backup Application Note, 80000NT10072A
- Telit UE HE910V2 DE CE910 HE920 DVI Application Note, 80000NT10101A
- Telit EVK2 User Guide, 1vv0300704

2. General Product Description

2.1. Overview

The aim of this document is the description of typical hardware solutions useful for developing a product with the Telit CE910-SL module.

In this document all the basic functions of a mobile device will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace all hardware solutions and products that may be designed. Avoiding the discussed wrong solutions must be considered as mandatory. While the suggested hardware configurations must not be considered mandatory, the information given must be used as a guide and a starting point for properly developing a product with the Telit CE910-SL module.

NOTE:

The integration of the CDMA 1xRTT module within a user application must be done according to the design rules described in this manual.

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2.2. Product Specifications

CE910-SL Specifications	
Air Interface	CDMA 1xRTT
Frequency Bands	CE910-SL : 450MHz, Block “C”
Data Service	CDMA 1xRTT: 153.6 Kbps (full-duplex)
Max. RF out power	• CDMA BC5: Power class 3 (24.5dBm) for 1xRTT
Typical conducted sensitivity	• CDMA BC5: –108dBm
Device dimensions	28.2mm(L) x 28.2mm(W) x 2.35mm(T)
Weight	About 3.6 g
Storage and Operating Temperature Range	–40 ~ +85°C
Normal operating voltage range	3.4 ~ 4.2V
IO voltage	1.8V
Interface	• 144 Land-Grid-Array interface • 10 general I/O ports maximum including multi-functional I/Os • State LED output • 1 A/D converter • Full RS232 CMOS UART: baud rate up to 4Mbps • Reserved two wires CMOS UART for debugging • USB 2.0: baud rate up to 12Mbps
Antenna	Primary antenna, 450MHz
Message	SMS (MO/MT)

2.3. Operating Frequency

The operating frequencies in CDMA450 (Band Class 5) mode are conformed to the 3GPP specifications.

Mode	Freq. TX (MHz)	Freq. RX (MHz)	Channels	TX - RX offset
CDMA450, Block “C” (4.8 MHz)	450.0 ~ 454.8	460.0 ~ 464.8	1 ~ 193	10 MHz

2.4. RoHS Compliance

As a part of Telit’s corporate policy of environmental protection, the CE910-SL complies with the RoHS (Restriction of Hazardous Substances) directive of the European Union (EU directive 2002/95/EG).

3. CE910-SL Module Connections

3.1. Pin-Out

Pin	Signal	I/O	Function	Type
USB FS 2.0 Communication Port				
B15	USB_D+	I/O	USB differential Data(+)	
C15	USB_D-	I/O	USB differential Data(-)	
A13	VUSB	I	Power for the internal USB transceiver	5V
Asynchronous UART – Prog. / data +HW Flow Control				
N15	C103/TXD	I	Serial data input from DTE	CMOS 1.8V
M15	C104/RXD	O	Serial data output to DTE	CMOS 1.8V
M14	C108/DTR	I	Input for (DTR) from DTE	CMOS 1.8V
L14	C105/RTS	I	Input for (RTS) from DTE	CMOS 1.8V
P15	C106/CTS	O	Output for (CTS) to DTE	CMOS 1.8V
N14	C109/DCD	O	Output for (DCD) to DTE	CMOS 1.8V
P14	C107/DSR	O	Output for (DSR) to DTE	CMOS 1.8V
R14	C125/RING	O	Output for (RI) to DTE	CMOS 1.8V
Asynchronous Auxiliary UART				
D15	TX_AUX	O	Auxiliary UART (TX Data to DTE)	CMOS 1.8V
E15	RX_AUX	I	Auxiliary UART (RX Data from DTE)	CMOS 1.8V
RUIM Interface(*NOTE)				
A3	SIMVCC	-	Reserved but applicable only to RUIM variant : Power supply for the RUIM	1.8/3V
A5	SIMIO	I/O	Reserved but applicable only to RUIM variant : RUIM Data I/O	1.8/3V
A6	SIMCLK	O	Reserved but applicable only to RUIM variant : RUIM Clock	1.8/3V
A7	SIMRST	O	Reserved but applicable only to RUIM variant : RUIM Reset	1.8/3V
Digital Voice interface				
B9	DVI_WA0	I/O	Digital Voice Interface (WA0)	CMOS 1.8V
B6	DVI_RX	I	Digital Voice Interface (RX)	CMOS 1.8V
B7	DVI_TX	O	Digital Voice Interface (TX)	CMOS 1.8V
B8	DVI_CLK	I/O	Digital Voice Interface (CLK)	CMOS 1.8V
Analog Voice Interface				
B2	EAR+	AO	Earphone signal output, phase +	
B3	EAR-	AO	Earphone signal output, phase -	
B4	MIC+	AI	Microphone input, phase +	
B5	MIC-	AI	Microphone input, phase -	
Digital IO				
C8	GPIO_01	I/O	GPIO_01 / STAT LED	CMOS 1.8V
C9	GPIO_02	I/O	GPIO_02	CMOS 1.8V
C10	GPIO_03	I/O	GPIO_03	CMOS 1.8V

Pin	Signal	I/O	Function	Type
C11	GPIO_04	I/O	GPIO_04	CMOS 1.8V
B14	GPIO_05	I/O	GPIO_05	CMOS 1.8V
C12	GPIO_06	I/O	GPIO_06	CMOS 1.8V
C13	GPIO_07	I/O	GPIO_07	CMOS 1.8V
K15	GPIO_08	I/O	GPIO_08	CMOS 1.8V
L15	GPIO_09	I/O	GPIO_09	CMOS 1.8V
G15	GPIO_10	I/O	GPIO_10	CMOS 1.8V
ADC Section				
B1	ADC_IN1	AI	Analog to Digital converter input	A/D
RF Section				
K1	Antenna	I/O	CDMA Antenna (50Ohm)	RF
Miscellaneous Functions				
R13	HW_SHUTDOWN*	I	Hardware Unconditional Shutdown	Pull up to VBATT
R12	ON_OFF*	I	Input Command for Power ON	CMOS 1.8V
C14	VRTC	I	RTC Power	Power
R11	VAUX/PWRMON	O	Supply Output for external accessories / Power ON Monitor	1.8V
Test Point				
C3	TP1		Test Point	TP
C4	TP2		Test Point	TP
C5	TP3		Test Point	TP
C6	TP4		Test Point	TP
C7	TP5		Test Point	TP
D3	TP6		Test Point	TP
E3	TP7		Test Point	TP
Power Supply				
M1	VBATT	-	Main Power Supply (Baseband)	Power
M2	VBATT	-	Main Power Supply (Baseband)	Power
N1	VBATT_PA	-	Main Power Supply (Radio PA)	Power
N2	VBATT_PA	-	Main Power Supply (Radio PA)	Power
P1	VBATT_PA	-	Main Power Supply (Radio PA)	Power
P2	VBATT_PA	-	Main Power Supply (Radio PA)	Power
E1	GND	-	Ground	
G1	GND	-	Ground	
H1	GND	-	Ground	
J1	GND	-	Ground	
L1	GND	-	Ground	
A2	GND	-	Ground	
E2	GND	-	Ground	
F2	GND	-	Ground	
G2	GND	-	Ground	
H2	GND	-	Ground	
J2	GND	-	Ground	
K2	GND	-	Ground	
L2	GND	-	Ground	
R2	GND	-	Ground	

Pin	Signal	I/O	Function	Type
M3	GND	-	Ground	
N3	GND	-	Ground	
P3	GND	-	Ground	
R3	GND	-	Ground	
D4	GND	-	Ground	
M4	GND	-	Ground	
N4	GND	-	Ground	
P4	GND	-	Ground	
R4	GND	-	Ground	
N5	GND	-	Ground	
P5	GND	-	Ground	
R5	GND	-	Ground	
N6	GND	-	Ground	
P6	GND	-	Ground	
R6	GND	-	Ground	
P8	GND	-	Ground	
R8	GND		Ground	
P9	GND	-	Ground	
P10	GND	-	Ground	
R10	GND	-	Ground	
M12	GND	-	Ground	
B13	GND	-	Ground	
P13	GND	-	Ground	
E14	GND	-	Ground	
Reserved				
C1	Reserved	-	Reserved	
D1	Reserved	-	Reserved	
F1	Reserved	-	Reserved	
C2	Reserved	-	Reserved	
D2	Reserved	-	Reserved	
F3	Reserved	-	Reserved	
G3	Reserved	-	Reserved	
H3	Reserved	-	Reserved	
J3	Reserved	-	Reserved	
K3	Reserved	-	Reserved	
L3	Reserved	-	Reserved	
A4	Reserved	-	Reserved	
N7	Reserved	-	Reserved	
P7	Reserved	-	Reserved	
R7	Reserved	-	Reserved	
A8	Reserved	-	Reserved	
N8	Reserved	-	Reserved	
A9	Reserved	-	Reserved	
N9	Reserved	-	Reserved	
R9	Reserved	-	Reserved	
A10	Reserved	-	Reserved	

Pin	Signal	I/O	Function	Type
B10	Reserved	-	Reserved	
N10	Reserved	-	Reserved	
A11	Reserved	-	Reserved	
B11	Reserved	-	Reserved	
N11	Reserved	-	Reserved	
P11	Reserved	-	Reserved	
A12	Reserved	-	Reserved	
B12	Reserved	-	Reserved	
D12	Reserved	-	Reserved	
N12	Reserved	-	Reserved	
P12	Reserved	-	Reserved	
D13	Reserved	-	Reserved	
E13	Reserved	-	Reserved	
F13	Reserved	-	Reserved	
G13	Reserved	-	Reserved	
H13	Reserved	-	Reserved	
J13	Reserved	-	Reserved	
K13	Reserved	-	Reserved	
L13	Reserved	-	Reserved	
M13	Reserved	-	Reserved	
N13	Reserved	-	Reserved	
A14	Reserved	-	Reserved	
D14	Reserved	-	Reserved	
F14	Reserved	-	Reserved	
G14	Reserved	-	Reserved	
H14	Reserved	-	Reserved	
J14	Reserved	-	Reserved	
K14	Reserved	-	Reserved	
F15	Reserved	-	Reserved	
H15	Reserved	-	Reserved	
J15	Reserved	-	Reserved	

WARNING:

Reserved pins must not be connected.

NOTE:

If not used, almost all pins not in use must be left disconnected. The only exceptions are the following pins:

PAD	Signal	Notes
M1,M2,N1,N2,P1,P2	VBATT&VBATT_PA	
E1,G1,H1,J1,L1,A2,E2,F2,G2,H2,J2,K2,L2,R2,M3,N3,P3,R3,D4,M4,N4,P4,R4,N5,P5,R5,N6,P6,R6,P8,R8,P9,P10,R10,M12,B13,P13,E14	GND	
R12	ON/OFF*	
R13	HW_SHUTDOWN*	
B15	USB_D+	If not used it should be connected to a Test point.
C15	USB_D-	If not used it should be connected to a Test point.
A13	VUSB	If not used it should be connected to a Test point.
N15	C103/TXD	If not used it should be connected to a Test point.
M15	C104/RXD	If not used it should be connected to a Test point.
L14	C105/RTS	If the flow control is not used it should be connected to GND.
P15	C106/CTS	If not used it should be connected to a Test point.
D15	TX_AUX	If not used it should be connected to a Test point.
E15	RX_AUX	If not used it should be connected to a Test point.
K1	Main Antenna	
C3,C4,C5,C6,C7,D3,E3	Test Point	

3.1.1. LGA Pads Layout(CE910-SL)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1		ADC_IN1	RES	RES	GND	RES	GND	GND	GND	ANTENNA	GND	VBATT	VBATT_PA	VBATT_PA		1
2	GND	EAR+	RES	RES	GND	GND	GND	GND	GND	GND	GND	VBATT	VBATT_PA	VBATT_PA	GND	2
3	RES	EAR-	TP1	TP6	TP7	RES	RES	RES	RES	RES	RES	GND	GND	GND	GND	3
4	RES	MIC+	TP2	GND								GND	GND	GND	GND	4
5	RES	MIC-	TP3										GND	GND	GND	5
6	RES	DVI_RX	TP4										GND	GND	GND	6
7	RES	DVI_TX	TP5										RES	RES	RES	7
8	RES	DVI_CLK	GPIO_01 / STAT_LED										RES	GND	GND	8
9	RES	DVI_WA0	GPIO_02										RES	GND	RES	9
10	RES	RES	GPIO_03										RES	GND	GND	10
11	RES	RES	GPIO_04										RES	RES	VAUX/PWRM ON	11
12	RES	RES	GPIO_06	RES								GND	RES	RES	ON_OFF*	12
13	VUSB	GND	GPIO_07	RES	RES	RES	RES	RES	RES	RES	RES	RES	RES	GND	HW_SHUTD OWN*	13
14	RES	GPIO_05	VRTC	RES	GND	RES	RES	RES	RES	RES	C105/RTS	C108/DTR	C109/DCD	C107/DSR	C125/RING	14
15		USB_D+	USB_D-	TX_AUX	RX_AUX	RES	GPIO_10	RES	RES	GPIO_08	GPIO_09	C104/RXD	C103/TXD	C106/CTS		15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Top View

NOTE:

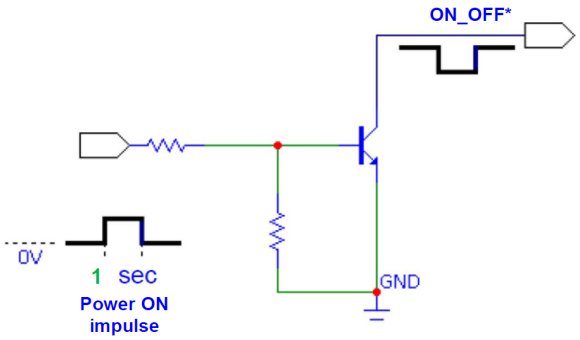
The pin defined as RES must be considered RESERVED and not connected on any pin in the application. The related area on the application has to be kept empty.

4. Hardware Commands

4.1. Turning on the CE910-SL module

To turn on the CE910-SL, the pad ON_OFF* must be tied low for at least 1.5 second and then released. The maximum current that can be drained from the ON_OFF* pad is 0.1 mA.

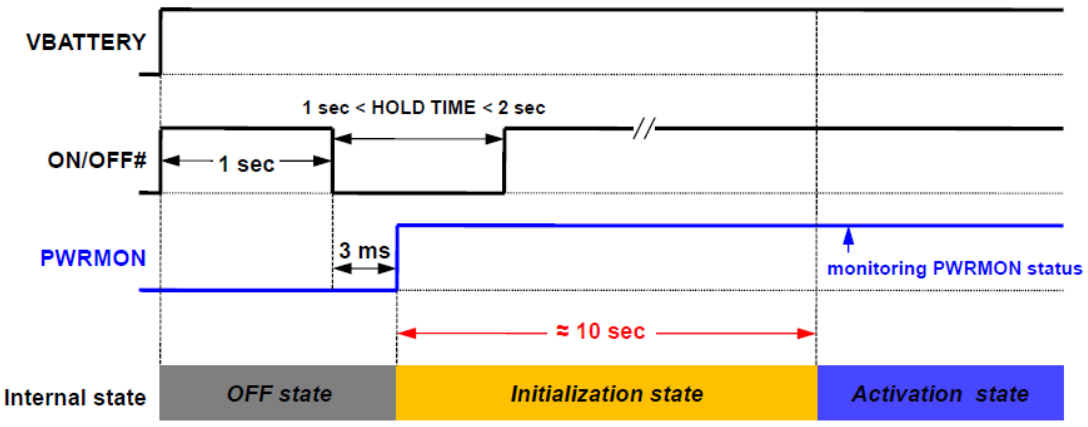
A simple circuit to power on the module is illustrated below:



4.1.1. Initialization and Activation State

Upon turning on CE910-SL module, the CE910-SL module is not active yet because the boot sequence of CE910-SL is still executing internally. It takes about 10 seconds to complete the initialization of the module internally.

For this reason, it would be useless to try to access CE910-SL during the Initialization state as below. The CE910-SL module needs at least 10 seconds after the PWRMON goes High to become operational by reaching the activation state.



During the *Initialization state*, any kind of AT-command is not available. DTE must wait for the *Activation state* to communicate with CE910-SL.

To check if the CE910-SL has powered on, the hardware line VAUX/PWRMON must be monitored. When VAUX/PWRMON goes high, the module has powered on.

NOTE:

Do not use any pull up resistor on the ON_OFF* line. It is pulled up with 200kΩ internally. Using a pull up resistor may bring latch up problems on the CE910-SL power regulator and improper power on/off of the module. The line ON_OFF* must be connected only in open collector configuration.

NOTE:

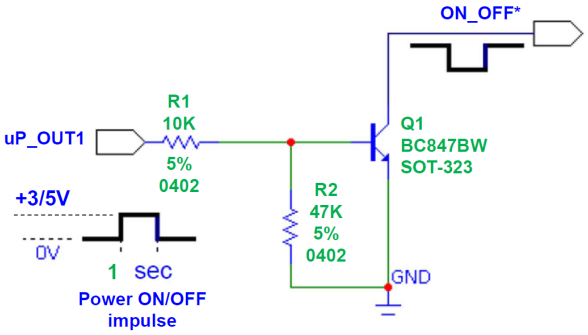
In this document all the lines are inverted. Active low signals are labeled with a name that ends with "*" or with a bar over the name.

NOTE:

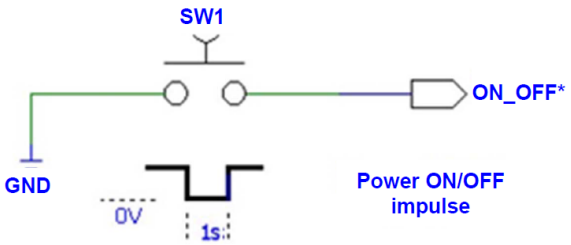
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CE910-SL module when the module is powered OFF or during an ON/OFF transition.

For example:

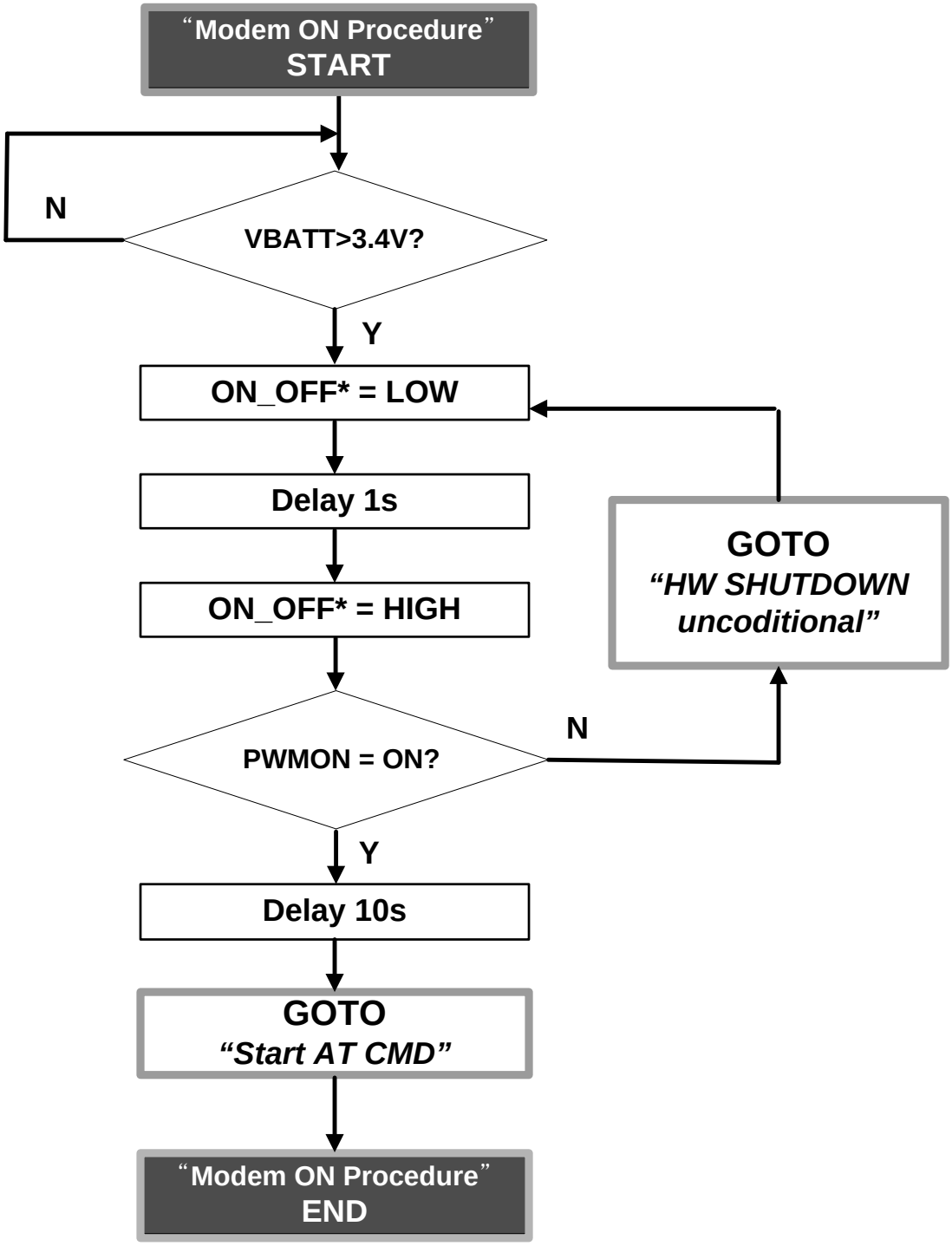
1. To drive the ON_OFF* pad with a totem pole output of a +3/5 V microcontroller (uP_OUT1):



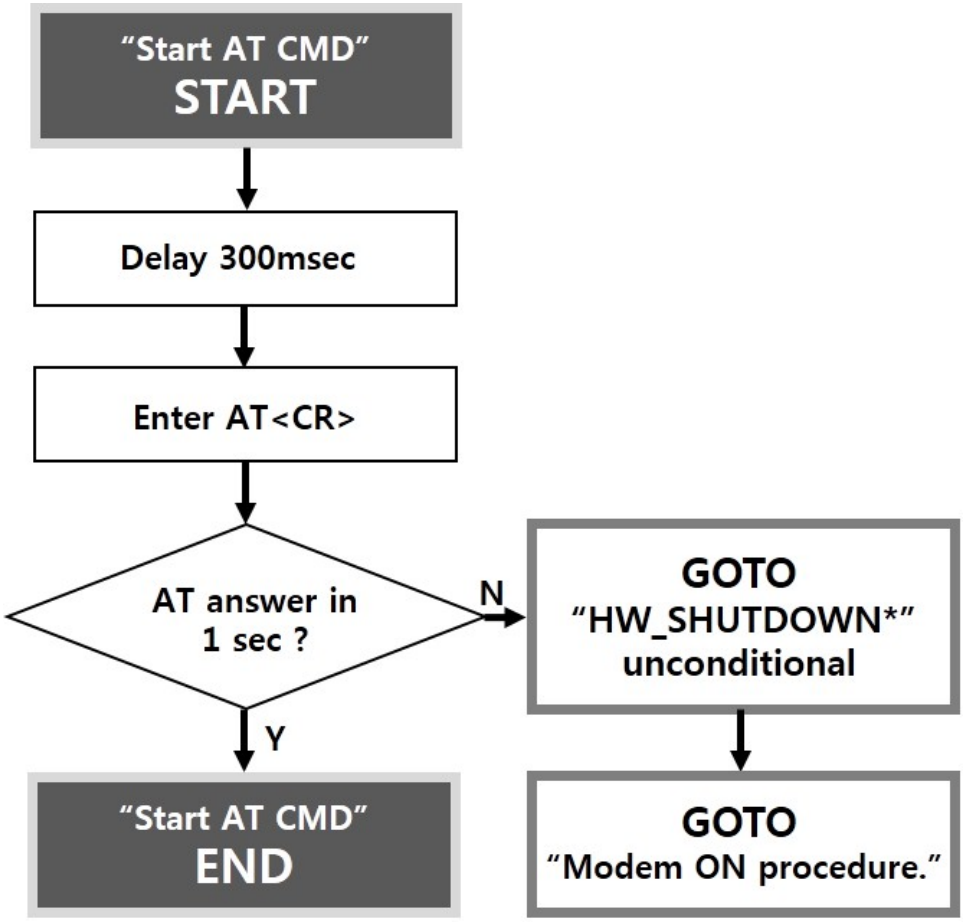
2. To drive the ON_OFF* pad directly with an ON/OFF button:



A flow chart the proper turn on procedure is displayed below:



A flow chart showing the AT commands managing procedure is displayed below:



4.2. Turning off the CE910-SL module

Turning off the device can be done in two ways:

- via AT command (see CE910-SL Software User Guide, AT#SHDN)
- by tying low pin ON_OFF*

Either ways, the device issues a detach request to network informing that the device will not be reachable any more.

To turn OFF the CE910-SL the pad ON_OFF* must be tied low for at least 2.5 seconds and then released.

TIP:

To check if the device has powered off, hardware line PWRMON must be monitored.

The device is powered off when PWRMON goes low.

NOTE:

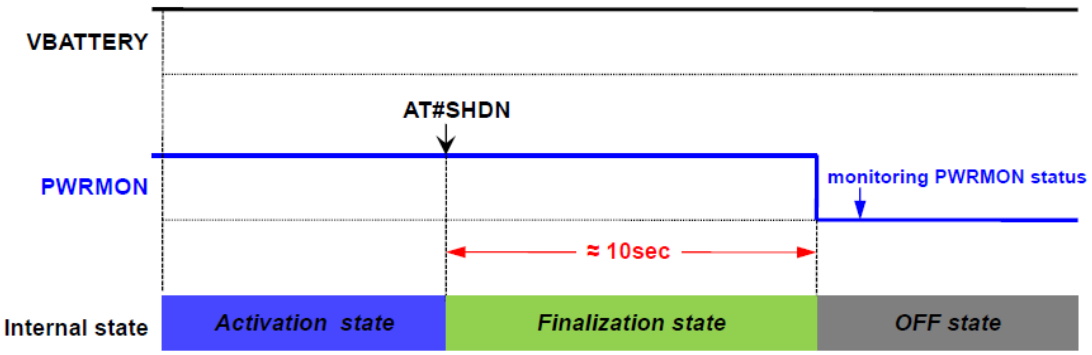
In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CE910-SL when the module is powered OFF or during an ON/OFF transition.

4.2.1. Turning OFF by AT Command

The CE910-SL can be shut down by a software command.

When a shutdown command is sent, the CE910-SL goes into the finalization state and will shut down PWRMON at the end of this state. The period of the finalization state can vary according to the state of the CE910-SL so it cannot be fixed definitely.

Normally it will be 10 seconds after sending a shutdown command and DTE should monitor the status of PWRMON to see the actual power off.



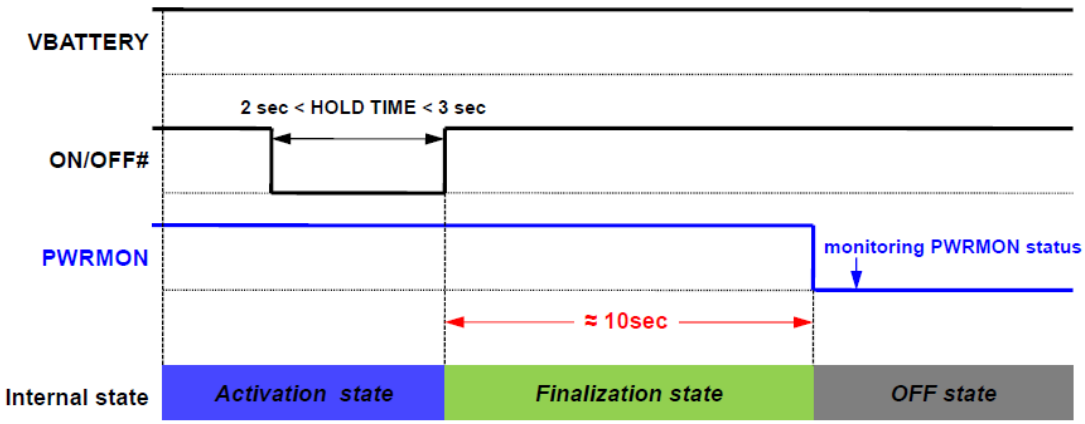
4.2.2. Turning OFF by tying low ON_OFF*

To turn OFF the CE910-SL the pad ON_OFF* must be tied low for at least 2 seconds and then released. The same circuitry and timing for the power on must be used.

When the hold time of ON_OFF* is above 2 seconds, the CE910-SL goes into the finalization state and will shut down PWRMON at the end of this state.

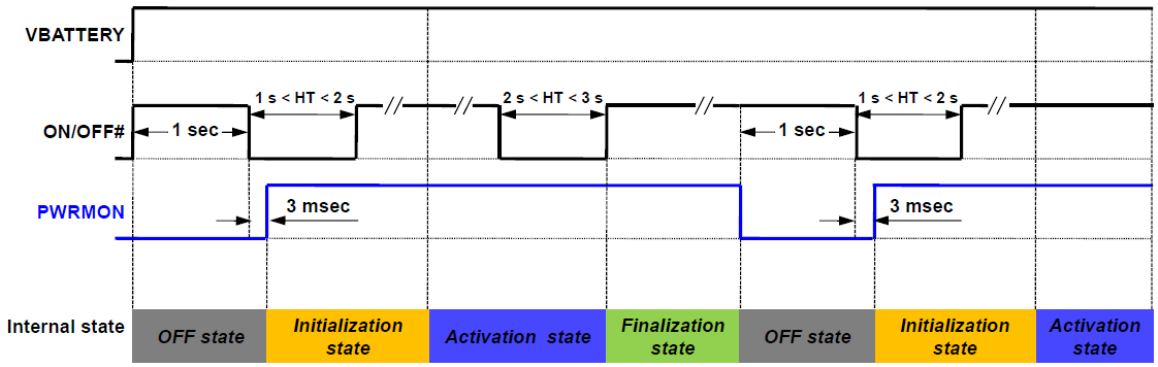
The period of the finalization state can vary according to the state of the CE910-SL so it cannot be fixed definitely.

Normally it will be 10 seconds after releasing ON_OFF* and DTE should monitor the status of PWRMON to see the actual power off.

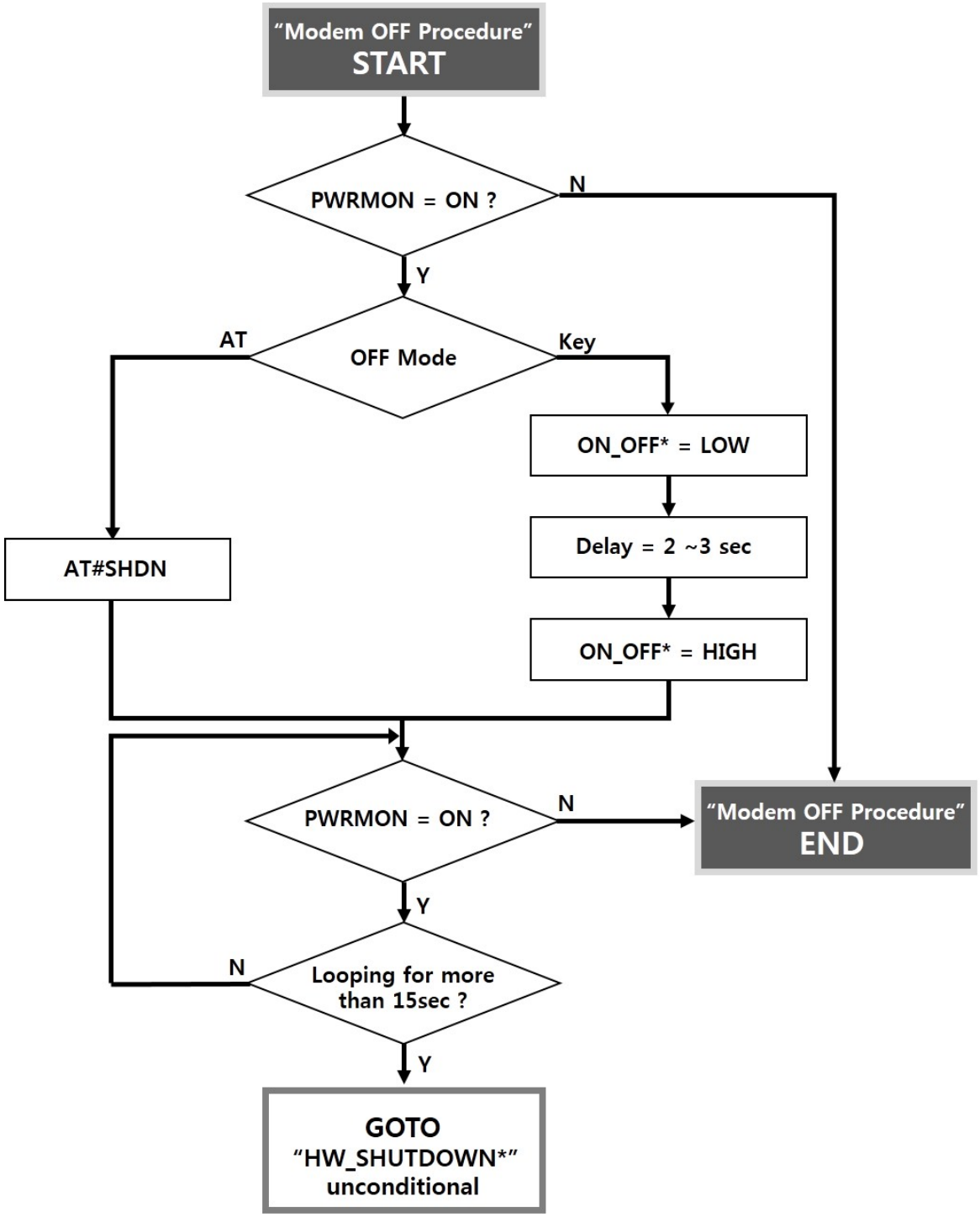


4.3. Summary of Turning ON and OFF the Module

The chart below describes the overall sequences for turning ON and OFF the module.



The following flow chart shows the proper turn off procedure:



4.4. Hardware Unconditional Shutdown

The Unconditional shutdown of the module could be activated using the HW_SHUTDOWN* line(pad R13).

WARNING:

The hardware unconditional shutdown must NOT be used during normal operation of the device since it does not detach the device from the network. It shall be used as an emergency exit procedure.

To unconditionally shutdown the CE910-SL, the pad HW_SHUTDOWN* must be tied low for at least 3.0 seconds and then released.

NOTE:

Do not use any pull up resistor on the HW_SHUTDOWN* line nor any totem pole digital output. It is pulled up internally to VBATT with 57kΩ. Using an external pull up resistor may bring latch up problems on the CE910-SL power regulator and improper functioning of the module.

The line HW_SHUTDOWN* must be connected only in open collector configuration.

The HW_SHUTDOWN* will generate an unconditional shutdown of the module without an automatic restart.

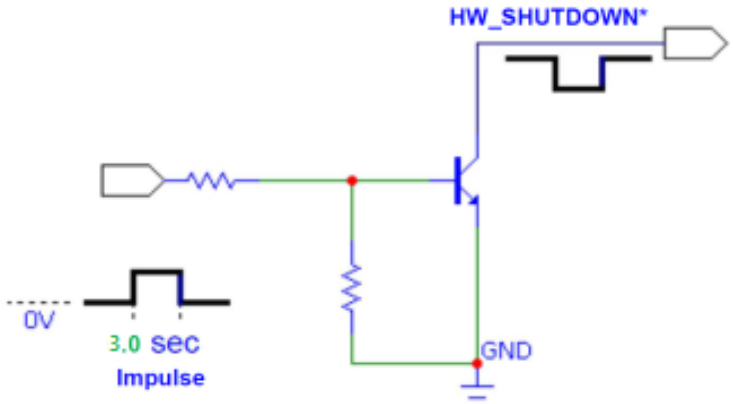
The module will shutdown but will NOT perform the detach from the cellular network.

To proper power on again the module please refer to 4.1 Turning ON the CE910-SL.

TIP:

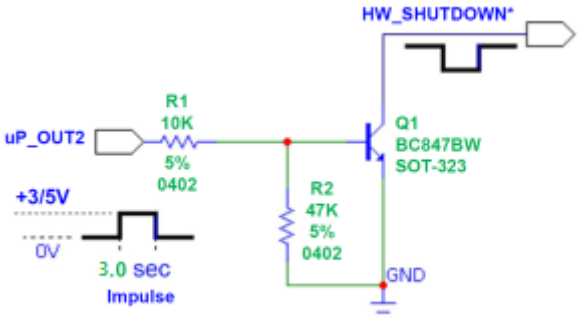
The unconditional hardware shutdown must always be implemented on the boards and the software must use it only as an emergency exit procedure.

A simple circuit to unconditionally shutdown the module is illustrated below:



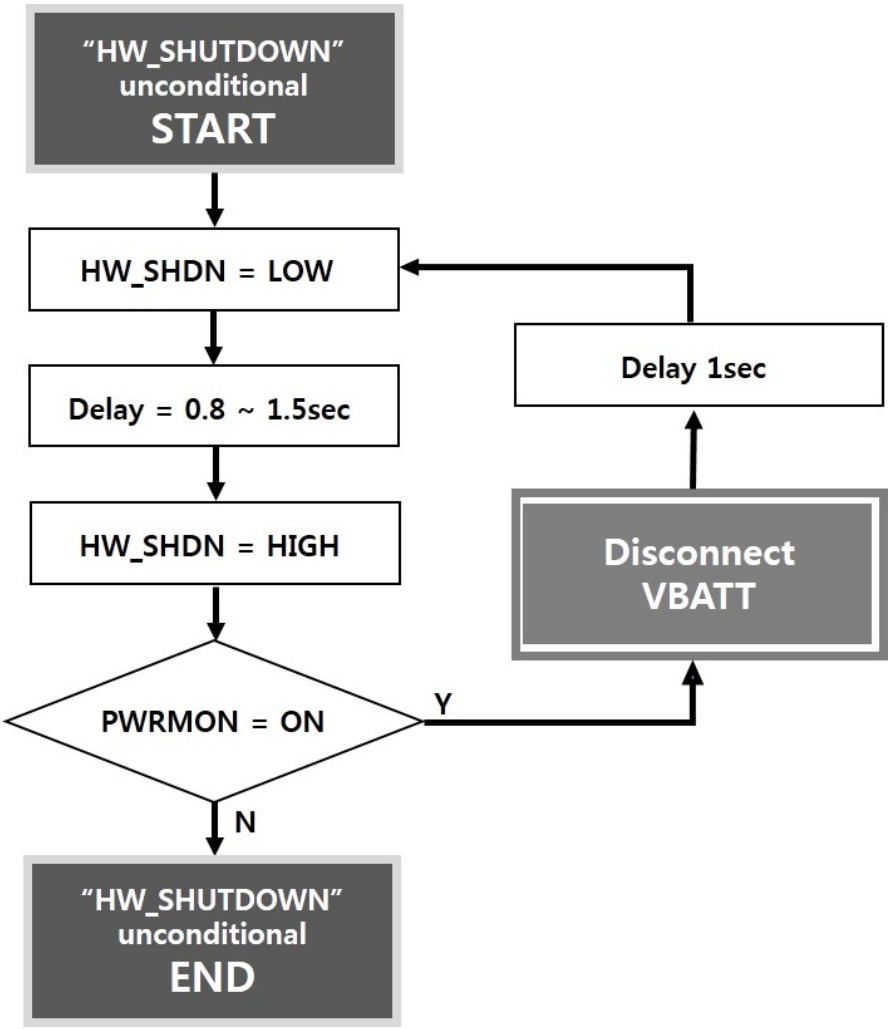
For example:

Let us assume you need to drive the HW_SHUTDOWN* pad with a totem pole output of a +3/5 V microcontroller (uP_OUT2):



NOTE: In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CE910-SL when the module is powered OFF or during an ON/OFF transition.

In the following flow chart is detailed the proper restart procedure:



5. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product's overall performance. Read carefully the requirements and the guidelines that follow for a proper design.

5.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfill the following requirements:

Power Supply	
Nominal Supply Voltage	3.8V
Normal Operating Voltage range	3.4V ~ 4.2V
Extended Operating Voltage range	3.4V ~ 4.5V

NOTE:

The Operating Voltage Range MUST never be exceeded. Special care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.

If the voltage drop is exceeding the limits it could cause a Power Off of the module.

5.2. Power Consumption

CE910-SL		
Mode	**Average (mA)**	**Mode Description**
Power off current (Typical)		71 uA(*1)
Standby mode		No call in progress (slot cycle index=2)
AT+CFUN=1	17.1	Normal mode; full functionality of the module
AT+CFUN=4	16.6	Disabled TX and RX; modules is not registered on the network
AT+CFUN=5	0.8(*2)	Full functionality with power saving; Module registered on the network can receive incoming call sand SMS
Tx and Rx mode		A call in progress
Max Power Mode	750	CDMA 1x voice/data call

(*1)The off current is the total supply current from the main battery with the XO regulator ON, 19.2MHz XO ON and others are OFF.
(*2) Standby current consumption depends on network configuration or module configuration. The current consumption value for CFUN= 5 is measured under slot cycle index=2.

TIP:

The electrical design for the power supply should be made ensuring it will be capable of a peak current output of at least 1A.

5.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout

5.3.1. Electrical Design Guidelines

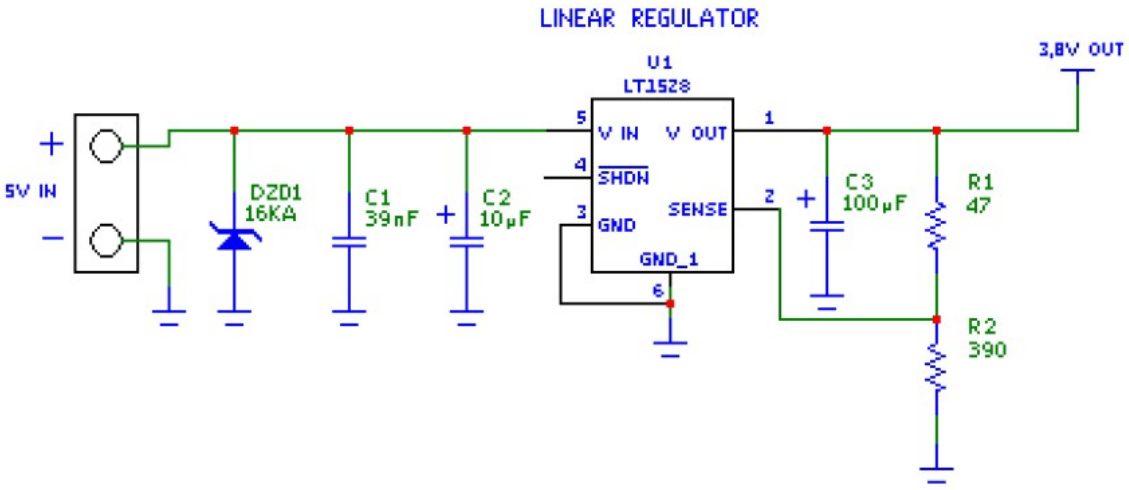
The electrical design of the power supply depends strongly on the power source where this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

5.3.2. + 5V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there is not a big difference between the input source and the desired output so a linear regulator can be used. A switching power supply will not be suitable because of the low drop-out requirements.
- When using a linear regulator, a proper heat sink must be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the CE910-SL. A 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the power input in order to save the CE910-SL from power polarity inversion.

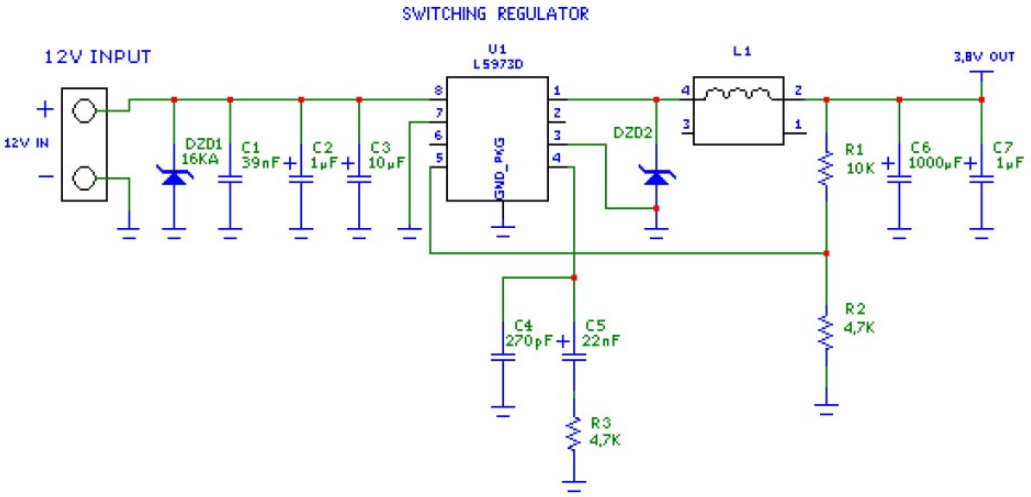
An example of a linear regulator with 5V input:



5.3.3. +12V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suitable and must not be used. A switching power supply would be preferable because of its better efficiency, especially with the 1A peak current load represented by CE910-SL.
- When using a switching regulator, a 500 kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case, the frequency and switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15.8V and this must be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks. A 100µF tantalum capacitor is usually suited for this.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For car applications a spike protection diode must be inserted close to the power input in order to clean the supply from spikes.
- A protection diode must be inserted close to the power input in order to save the CE910-SL from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the schematic below:



5.3.4. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V. A single 3.7V lithium-ion cell battery type is ideal to supply power to the Telit CE910-SL module.

WARNING:

The three battery cells (Ni/Cd or Ni/MH 3.6V nom. battery types or 4V PB types) MUST NOT be used directly because their maximum voltage can rise over the absolute maximum voltage for the CE910-SL and cause damage. USE only Li-Ion battery types.

- A bypass low (usually a 100uF tantalum) ESR capacitor with adequate capacity must be provided in order to cut the current absorption peaks.
- Make sure the low ESR capacitor (usually a tantalum) is rated at least 10V.
- A protection diode must be inserted close to the power input in order to protect the CE910-SL module from power polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 1A. The suggested battery capacity is from 500mAh to 1000mAh.

5.3.5. Thermal Design Guidelines

The thermal design for the power supply heat sink must be done with the following specifications:

Average current consumption during CDMA 1x @PWR level max : 750 mA

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit via the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

If we assume that the device stays in transmission for short periods of time (a few minutes) and then remains for quite a long time in idle (one hour), then the power supply always has time to cool down between the calls and the heat sink could be smaller than the calculated for 750mA maximum RMS current. There could even be a simple chip package (no heat sink).

Moreover in average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than 750 mA (usually around 300 mA).

For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.

The heat generated by the CE910-SL must be taken into consideration during transmission at 24.5dBm max during calls. This generated heat will be mostly conducted to the ground plane under the CE910-SL. The application must be able to dissipate heat.

In the CDMA 1x mode, since CE910-SL emits RF signals continuously during transmission, special attention must be paid to how to dissipate the heat generated.

The current consumption will be up to about 750mA in CDMA 1x continuously at the maximum TX output power (24.5dBm). Thus, you must arrange the area on the application PCB must be as large as possible under CE910-SL.

The CE910-SL must be mounted on the large ground area of the application board and make many ground vias to dissipate the heat.

5.3.6. Power Supply PCB layout Guidelines

As seen in the electrical design guidelines, the power supply must have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct operation of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The bypass low ESR capacitor must be placed close to the Telit CE910-SL power input pads, or if the power supply is a switching type, the capacitor can be placed close to the inductor to cut the ripple if the PCB trace from the capacitor to CE910-SL is wide enough to ensure a drop-less connection even during the 1A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 1A current peaks are absorbed. While a voltage drop of hundreds of mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If the application does not have an audio interface but only uses the data feature of the Telit CE910-SL, then this noise is not as disruptive and the power supply layout design can be more forgiving.

- The PCB traces to CE910-SL and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 1A current peaks are absorbed. This is a must for the same above-mentioned reasons. Try to keep this trace as short as possible.
- The PCB traces connecting the switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (usually 100-500 kHz).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board must be done in a way to guarantee that the high current return paths in the ground plane are not overlapped with any noise sensitive circuitry such as the microphone amplifier/buffer or earphone amplifier.

The power supply input cables must be kept separate from noise sensitive lines such as microphone/earphone cables.

6. Antenna

The antenna connection and board layout design are the most important parts in the full product design and they strongly reflect on the product's overall performance. Read carefully and follow the requirements and the guidelines for a proper design.

6.1. CDMA Antenna Requirements

The antenna for a Telit CE910-SL device must fulfill the following requirements:

CE910-SL Specifications	
Frequency range	Depending on the frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s)
Bandwidth	5 MHz in CDMA BC5
Impedance	50 Ohm
Input power	> 24.5dBm Average Power in CDMA
VSWR absolute max	≤ 5:1 (Limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (Limit to fulfill all regulatory requirement)

When using the Telit CE910-SL, since there's no antenna connector on the module, the antenna must be connected to the CE910-SL antenna pad (K1) by means of a transmission line implemented in the PCB.

In the case that the antenna is not directly connected at the antenna pad of the CE910-SL, then a PCB line is required. This transmission line shall fulfill the following requirements:

Antenna Line on PCB Requirements	
Characteristic Impedance	50Ohm
Max Attenuation	0.3dB
Coupling with other signals shall be avoided	
Cold End (Ground Plane) of antenna shall be equipotential to the CE910-SL ground pads	

Furthermore if the device is developed for the US and/or Canada market, it must comply with the FCC and/or IC approval requirements:

This device is to be used only for mobile and fixed application. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-Users must be provided with transmitter operation conditions for satisfying RF exposure compliance. OEM integrators must ensure that the end user has no manual instructions to remove or install the CE910-

SL module. Antennas used for this OEM module must not exceed 5dBi gain for mobile and fixed operating configurations.

6.2. CDMA antenna – PCB line Guidelines

- Make sure that the transmission line's characteristic impedance is 50ohm.
- Keep line on the PCB as short as possible since the antenna line loss shall be less than around 0.3dB.
- Line geometry should have uniform characteristics, constant cross section, avoid meanders and abrupt curves.
- Any kind of suitable geometry/structure can be used for implementing the printed transmission line afferent the antenna.
- If a Ground plane is required in line geometry, that plane has to be continuous and sufficiently extended so the geometry can be as similar as possible to the related canonical model.
- Keep, if possible, at least one layer of the PCB used only for the Ground plane; If possible, use this layer as reference Ground plane for the transmission line.
- It is wise to surround (on both sides) the PCB transmission line with Ground. Avoid having other signal tracks facing directly the antenna line track.
- Avoid crossing any un-shielded transmission line footprint with other tracks on different layers.
- The Ground surrounding the antenna line on PCB has to be strictly connected to the main Ground plane by means of via holes (once per 2mm at least) placed close to the ground edges facing line track.
- Place EM noisy devices as far as possible from CE910-SL antenna line.
- Keep the antenna line far away from the CE910-SL power supply lines.
- If EM noisy devices are present on the PCB hosting the CE910-SL, such as fast switching ICs, take care of shielding them with a metal frame cover.
- If EM noisy devices are not present around the line use of geometries like Micro strip or Grounded Coplanar Waveguide are preferred since they typically ensure less attenuation when compared to a Strip line having same length.

6.3. CDMA Antenna installation Guidelines

- Install the antenna in a place covered by the CDMA signal.
- If the device antenna in the application is located greater then 20cm from the human body and there are no co-located transmitters then the Telit FCC/IC approvals can be re-used by the end product.
- Antenna shall not be installed inside metal cases.
- Antenna shall be installed also according to antenna manufacture instructions.

WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect CE910-SL or customer specific requirements from ESD event to Antenna port (K1).

7. USB Port

The CE910-SL module includes a Universal Serial Bus (USB) transceiver, which operates at USB Full-speed (12Mbits/sec) and slave mode only.

It is compliant with the USB 2.0 specification and can be used for diagnostic monitoring, control and data transfers.

The table below describes the USB interface signals:

Pin	Signal	I/O	Function	Type
B15	USB_D+	I/O	USB differential Data(+)	
C15	USB_D-	I/O	USB differential Data(-)	
A13	VUSB	I	Power for the internal USB transceiver	5V

The USB_DPLUS and USB_DMINUS signals have a clock rate of 60MHz. The signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized. The impedance value should be as close as possible to 100 Ohms differential.

The table below describes the VUSB specification:

Parameter	Min	Max
Input voltage	4.4V	5.0V
Input current	50mA	-

WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect CE910-SL or customer specific requirements from ESD event to USB lines (B15, C15 and A13).

8. Serial Port

The serial port on the Telit CE910-SL is the interface between the module and OEM hardware.

1 serial port is available on the module:

- Modem Serial Port 1 (Main)

Several configurations can be designed for the serial port on the OEM hardware.

The most common are:

- RS232 PC comport
- Microcontroller UART@1.8V(Universal Asynchronous Receiver Transmit)
- Microcontroller UART@5V or other voltages different from 1.8V

Depending on the type of serial port on the OEM hardware, a level translator circuit may be needed to make the system work.

On the CE910-SL the ports are CMOS 1.8V.

The electrical characteristics of the serial port are explained in the following tables:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on non-power pin with respect to ground	-0.3	+2.3V

Operating Range - Interface levels (1.8V CMOS)

Parameter	Min	Max
Input high level	1.5V	2.1 V
Input low level	0V	0.35V
Output high level	1.35V	1.8V
Output low level	0V	0.45V

8.1. Modem Serial Port 1

The serial port 1 on the CE910-SL is a +1.8V UART with all 7 RS232 signals.

It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

RS232 Pin #	Signal	CE910-SL Pad No.	Function	Usage
1	C109/DCD	N14	Data Carrier Detect	Output from the CE910-SL that indicates the carrier presence
2	C104/RXD	M15	Transmit line *see Note	Output transmit line of the CE910-SL UART
3	C103/TXD	N15	Receive line *see Note	Input receive of the CE910-SL UART
4	C108/DTR	M14	Data Terminal Ready	Input to the CE910-SL that controls the DTE READY condition
5	GND	-	-	GND
6	C107/DSR	P14	Data Set Ready	Output from the CE910-SL that indicates the module is ready
7	C106/CTS	P15	Request to Send	Output from the CE910-SL that controls the hardware flow control
8	C105/RTS	L14	Clear to Send	Input to the CE910-SL that controls the hardware flow control
9	C125/RI	R14	Ring Indicator	Output from the CE910-SL that indicates the incoming call condition

The following table shows the typical value (pulled inside the baseband chipset) and status for input lines in all module states:

Signal/State	OFF	RESET	ON	Powersaving	PU tied to
TXD	unknown	Pull Down (21K~210K)	Pull Up (39K~390K)	Pull Up (39K~390K)	1.8V
RTS		Pull Down (21K~210K)			
DTR		Pull Up (39K~390K)			

NOTE:

According to V.24, RX/TX signal names are referred to the application side. Therefore, on the CE910-SL side these signals are on the opposite direction:

TXD on the application side will be connected to the receive line (here named C103/TXD)

RXD in the application side will be connected to the transmit line (here named C104/RXD)

NOTE:

For minimum implementation, only the TXD and RXD lines must be connected, the other lines can be left open provided a software flow control is implemented.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CE910-SL when the module is powered off or during an ON/OFF transition.

NOTE:

High-speed UART supports up to 4Mbps. Please refer to the AT command User Guide in detail.

WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect CE910-SL or customer specific requirements from ESD event to UART port (M15, N15, P15 and L14).

8.2. RS232 Level Translation

In order to interface the Telit CE910-SL with a PC com port or a RS232 (EIA/TIA-232) application, a level translator is required. This level translator must:

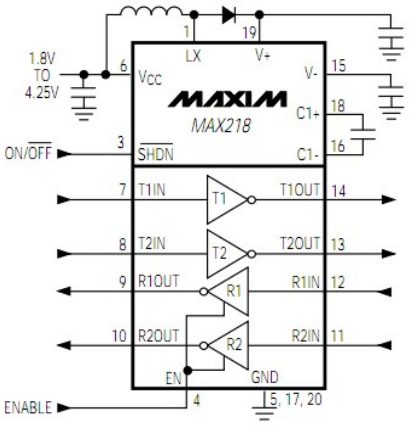
- Invert the electrical signal in both directions
- Change the level from 0/1.8V to +/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required. The simplest way to translate the levels and invert the signal is by using a single chip level translator. There is a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards). By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.

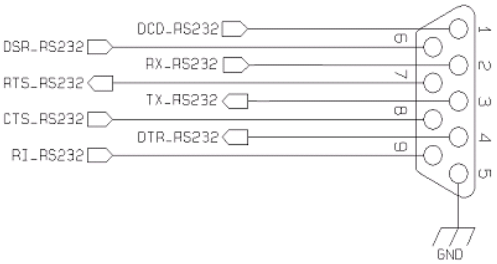
In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers

An example of RS232 level adaption circuitry could be accomplished using a MAXIM transceiver (MAX218). In this case the chipset is capable of translating directly from 1.8V to the RS232 levels (Example on 4 signals only).



The RS232 serial port lines are usually connected to a DB9 connector with the following layout:


DCD_RS232
DSR_RS232
RX_RS232
RTS_RS232
TX_RS232
CTS_RS232
DTR_RS232
RI_RS232
1
6
2
7
3
8
4
9
5
GND

9. Audio Section Overview

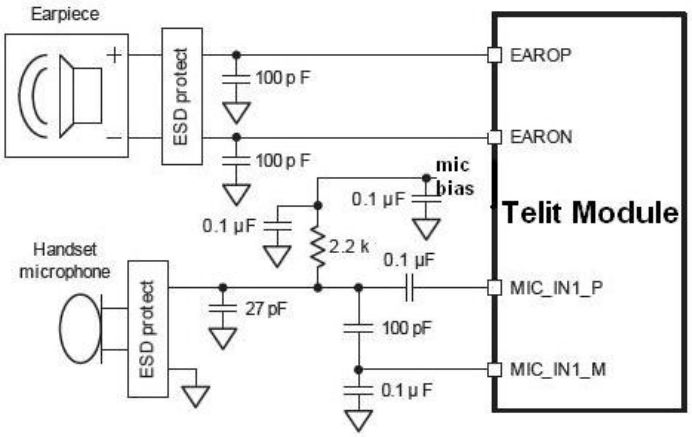
The CE910-SL provides an analog audio interface and digital audio interface.

9.1. Analog Audio Interface(AVI)

The CE910-SL provides an analog audio interface; one differential input for audio to be transmitted(Uplink) and a balanced output for audio to be received(Downlink).

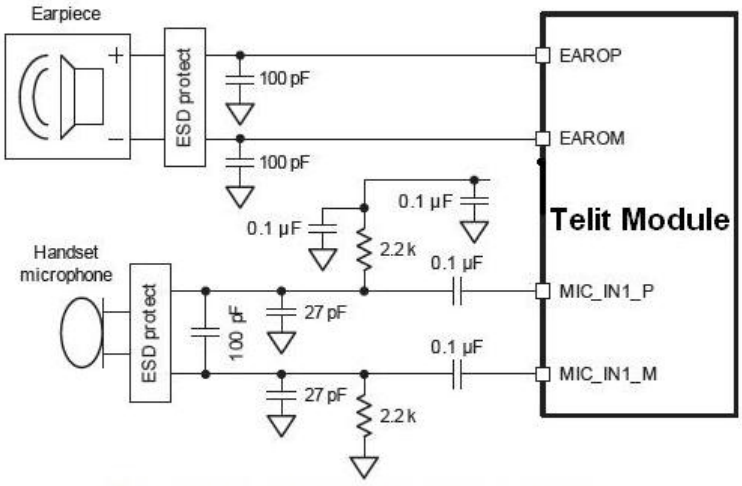
The bias for the microphone has to be as clean as possible; the first connection (single ended) is preferable since the Vmic noise and ground noise are fed into the input as common mode and then rejected. This sounds strange; usually the connection to use in order to reject the common mode is the balanced one. In this situation we have to recall that the microphone is a sound to current transducer, so the resistor is the current to tension transducer, so finally the resistor feeds the input in balanced way even if the configuration, from a microphone point of view, seems to be un-balanced.

9.1.1. MIC Connection



Single-ended microphone connection

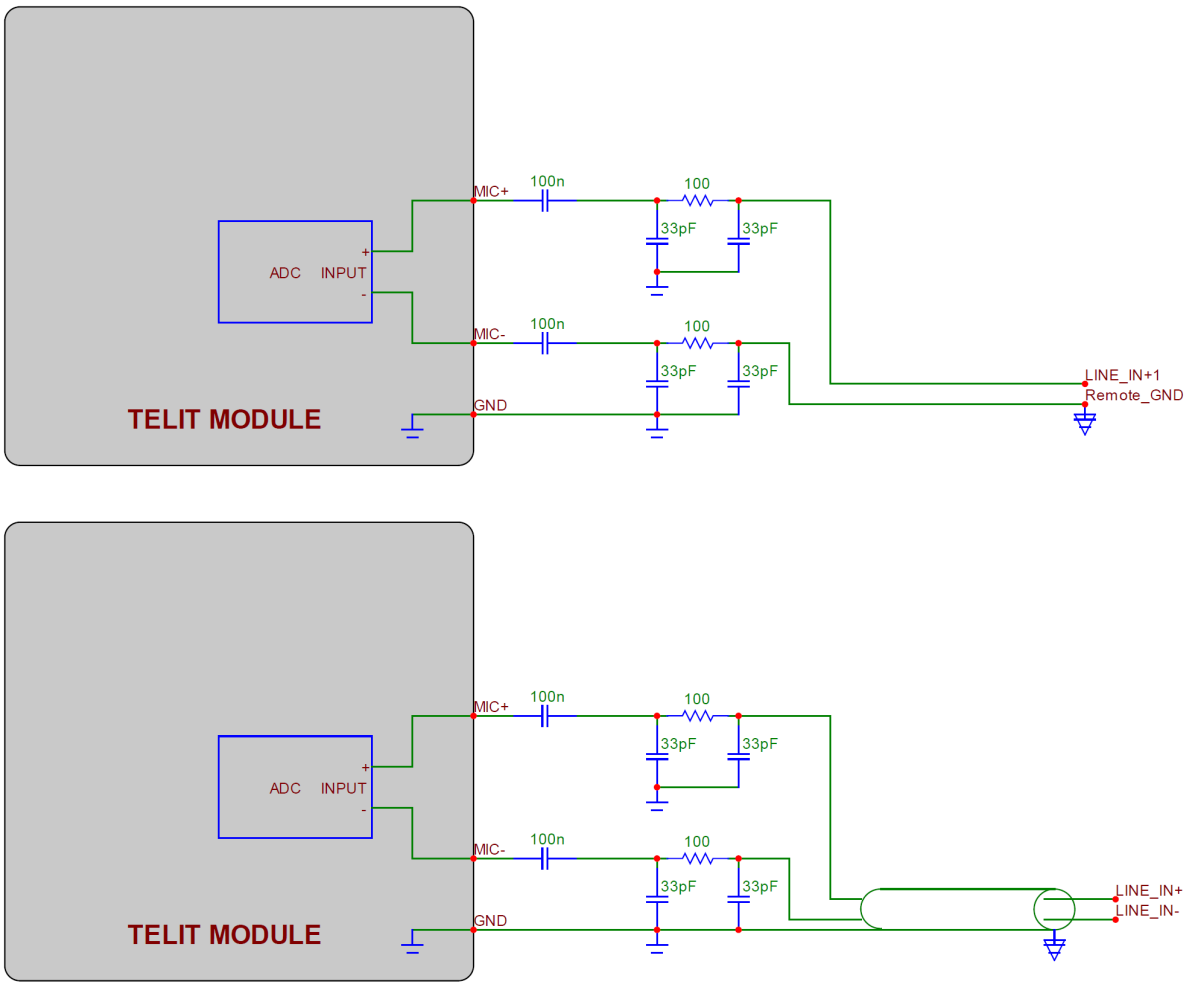
If a “balanced way” is anyway desired, much more care has to be taken to VMIC noise and ground noise.



Differential microphone connection

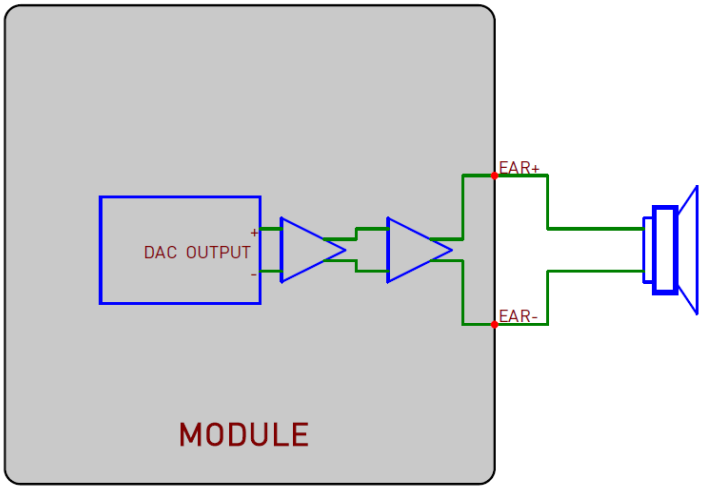
TIP: Since the J-FET transistor inside the microphone acts as RF-detector-amplifier, ask vendor for a microphone with anti-EMI capacitor (usually a 33pF or a 10pF capacitor placed across the output terminals inside the case).

9.1.2. LIN-IN Connection



If the audio source is not a mike but a different device, the following connections can be done. Place 100nF capacitor in series with both inputs, so the DC current is blocked. Place the 33pF-100Ohm-33pF RF-filter, in order to prevent some EMI field to get into the high impedance high gain MIC inputs. Since the input is differential, the common mode voltage noise between the two (different) grounds is rejected, provided that both AF_IN+ & AF_IN- are connected directly onto the source.

9.1.3. EAR Connection



The audio output of the CE910-SL is balanced, this is helpful to double the level and to reject common mode (click and pop are common mode and therefore rejected). These outputs can drive directly a small loudspeaker with electrical impedance not lower than 32Ohm.

TIP: in order to get the maximum audio level at a given output voltage level (dBspl/Vrms), the following breaking through procedure can be used. Have the loudspeaker as close as you can to the listener (this simplify also the echo cancelling); choose the loudspeaker with the higher sensitivity (dBspl per W); choose loudspeakers with the impedance close to the limit in order to feed more power inside the transducer (it increases the W/Vrms ratio). If this were not enough, an external amplifier should be used.

9.2. Digital Voice Interface(DVI)

The product is providing one Digital Audio Interface (DVI) on the following Pins:

Pin	Signal	I/O	Function	Type
B9	DVI_WA0	I/O	Digital Voice interface (WA0)	1.8V
B6	DVI_RX	I	Digital Voice interface (RX)	
B7	DVI_TX	O	Digital Voice interface (TX)	
B8	DVI_CLK	I/O	Digital Voice interface (CLK)	

9.2.1. CODEC Example

Please refer to the Telit UE HE910V2 DE CE910 HE920 DVI Application Note.

10. General Purpose I/O

The CE910-SL module is provided by a set of Digital Input / Output pins

Input pads can only be read; they report the digital value (high or low) present on the pad at the read time.

Output pads can only be written or queried and set the value of the pad output.

An alternate function pad is internally controlled by the CE910-SL firmware and acts depending on the function implemented.

The following GPIOs are available on the CE910-SL:

Pin	Signal	I/O	Function	Type	Default State	Note
C8	GPIO_01	I/O	Configurable GPIO	CMOS 1.8V	INPUT	Alternate function STAT_LED
C9	GPIO_02	I/O	Configurable GPIO	CMOS 1.8V	INPUT	
C10	GPIO_03	I/O	Configurable GPIO	CMOS 1.8V	INPUT	
C11	GPIO_04	I/O	Configurable GPIO	CMOS 1.8V	INPUT	
B14	GPIO_05	I/O	Configurable GPIO	CMOS 1.8V	INPUT	
C12	GPIO_06	I/O	Configurable GPIO	CMOS 1.8V	INPUT	
C13	GPIO_07	I/O	Configurable GPIO	CMOS 1.8V	INPUT	
K15	GPIO_08	I/O	Configurable GPIO	CMOS 1.8V	INPUT	
L15	GPIO_09	I/O	Configurable GPIO	CMOS 1.8V	INPUT	
G15	GPIO_10	I/O	Configurable GPIO	CMOS 1.8V	INPUT	

10.1. Logic Level Specification

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels.

The following table shows the logic level specifications used in the CE910-SL interface circuits:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.3V

Operating Range - Interface levels (1.8V CMOS)

Parameter	Min	Max
Input high level	1.5V	2.1V
Input low level	0.0V	0.35V
Output high level	1.35V	1.8V
Output low level	0.0V	0.45V

Current characteristics

Parameter	Typical
Output Current	2mA
Input Current	30uA

10.2. Using a GPIO Pad as Input

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47KΩ pull-up resistor to 1.8V.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

10.3. Using a GPIO Pad as Output

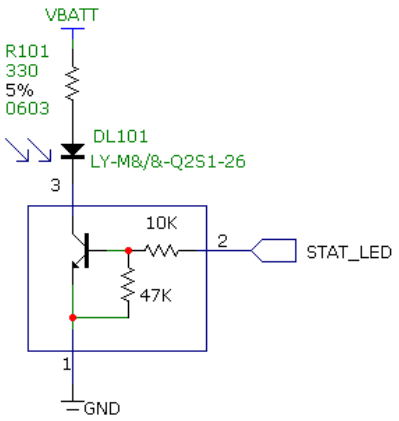
The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

10.4. Indication of Network Service Availability

The STAT_LED pin status shows information on the network service availability and Call status. In the CE910-SL modules, the STAT_LED usually needs an external transistor to drive an external LED. Because of the above, the status indicated in the following table is reversed with respect to the pin status:

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active

A schematic example could be:



10.5. RTC Bypass Output

The VRTC pin brings out the Real Time Clock supply but it is NOT separate from the rest of the digital part. So unlike other Telit's products, CE910-SL series cannot support RTC function if VBATT is not supplied. In this reason xE910 RTC Backup Application Note is NOT valid for CE910-SL.

In summary in order to use RTC function with CE910-SL, VBATT must be supplied from the application.

VRTC also supplies reference power to help CE910-SL check the time from SMPL (Sudden Momentary Power Loss).

So it is recommended as best practice to connect VRTC to a shunt capacitor (VRTC to GND) and the acceptable capacitor value is:

Parameter	Min
Keep-alive capacitor on Pad no. = C14	6.8uF

NOTE:

VBATT must be supplied in order to use RTC function.

NOTE:

It is recommended to add a keep-alive capacitor on VRTC.

WARNING:

NO devices must be powered from this pin.

10.6. VAUX/PWRMON Power Output

A regulated power supply output is provided in order to supply small devices from the module. This output is active when the module is ON and goes OFF when the module is shut down. The operating range characteristics of the supply are:

Operating Range – VAUX/PWRMON power supply

Parameter	Min	Typical	Max
Output voltage	1.77V	1.8V	1.83V
Output current			200mA
Output bypass capacitor (Inside the module)		2.2µF	

11. ADC section

11.1. Description

The on board ADC is 12-bit converter. It is able to read a voltage level in the range of 0 ~ 1.2 volts applied on the ADC pin input and store and convert it into 12 bit word.

Parameter	Min	Max	Units
Input Voltage range	0	1.2	Volt
AD conversion	-	12	bits
Resolution	-	< 1	mV
Input Resistance	1		Mohm

The CE910-SL provides one Analog to Digital Converter.

The input line is named as ADC_IN1 and it is available on pad B1.

11.2. Using ADC Converter

An AT command is available to use the ADC function.

The command is AT#ADC=1,2. The read value is expressed in mV

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

WARNING:

The ADC value read by AT command may present a certain level when it's open(not loaded). It is not an actual error and the ADC value is valid only if any input is asserted to ADC_IN1

12. Test Point

These pins are needed in order to analyze CE910-SL on the application board.

The signals of the CE910-SL are:

PAD	Signal	I/O	Function	Type
C3	TP1		Test Point	TP
C4	TP2		Test Point	TP
C5	TP3		Test Point	TP
C6	TP4		Test Point	TP
C7	TP5		Test Point	TP
D3	TP6		Test Point	TP
E3	TP7		Test Point	TP

13. Mounting CE910-SL on the Application

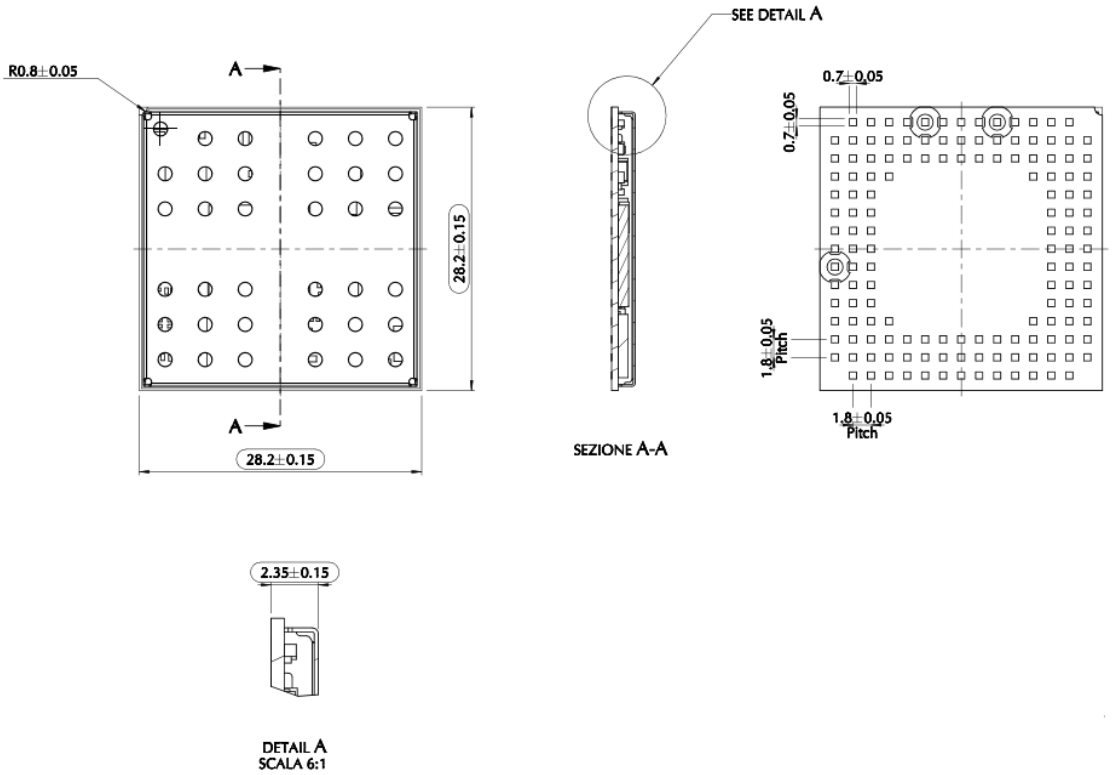
13.1. General

The CE910-SL has been designed in order to be compliant with a standard lead-free SMT process.

13.2. Module Finishing & Dimensions

The CE910-SL overall dimensions are:

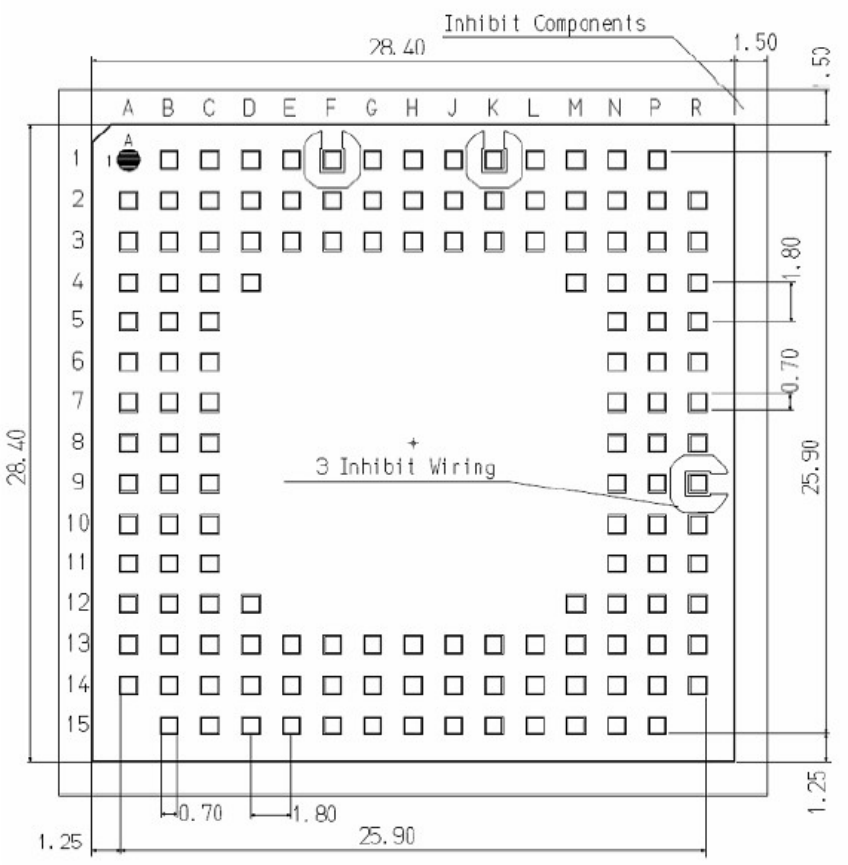
- Length : 28.2 mm
- Width : 28.2 mm
- Thickness : 2.35 mm
- Weight : about 3.6 g



Top view Bottom view

(Dimensions in mm)

13.3. Recommended foot print for the application



144 pins

< Top View >

In order to easily rework the CE910-SL it is suggested to consider having a 1.5 mm placement inhibit area around the module on the application.

It is also suggested, as a common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

NOTE:

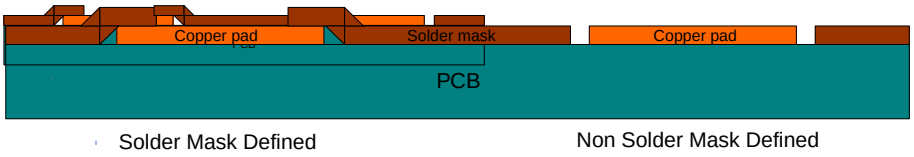
In the customer application, the region under WIRING INHIBIT (see figure) must be clear from signal or ground paths.

13.4. Stencil

Stencil's apertures layout can be the same as the recommended footprint (1:1). A suggested thickness of stencil foil ≥ 120 µm.

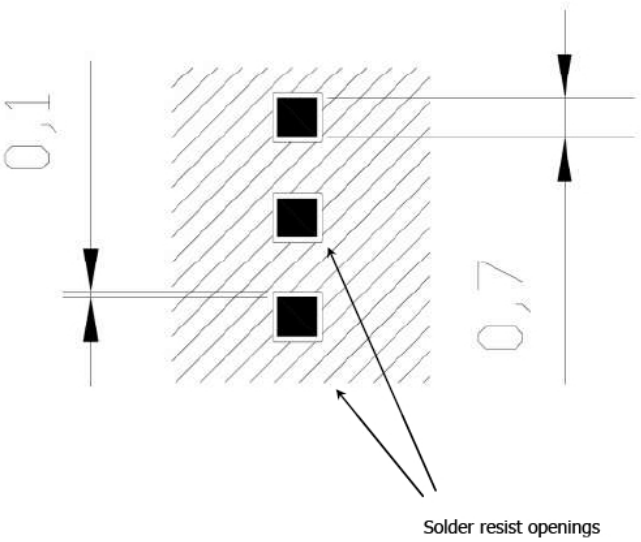
13.5. PCB Pad Design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

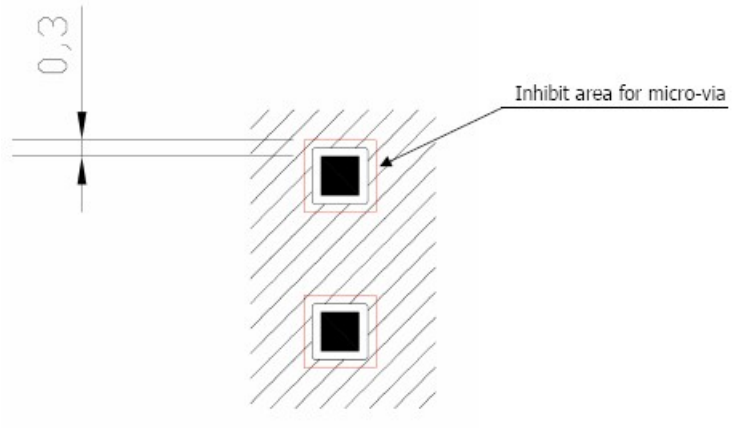


13.6. Recommendations for PCB Pad Dimensions (mm)

The recommendation for the PCB pads dimensions are described in the following image(dimensions in mm)



It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal as the pad itself (see following figure).



Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB Pad Surfaces:

Finish	Layer thickness (um)	Properties
Electro-less Ni / Immersion Au	3 ~ 7 / 0.05 ~ 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

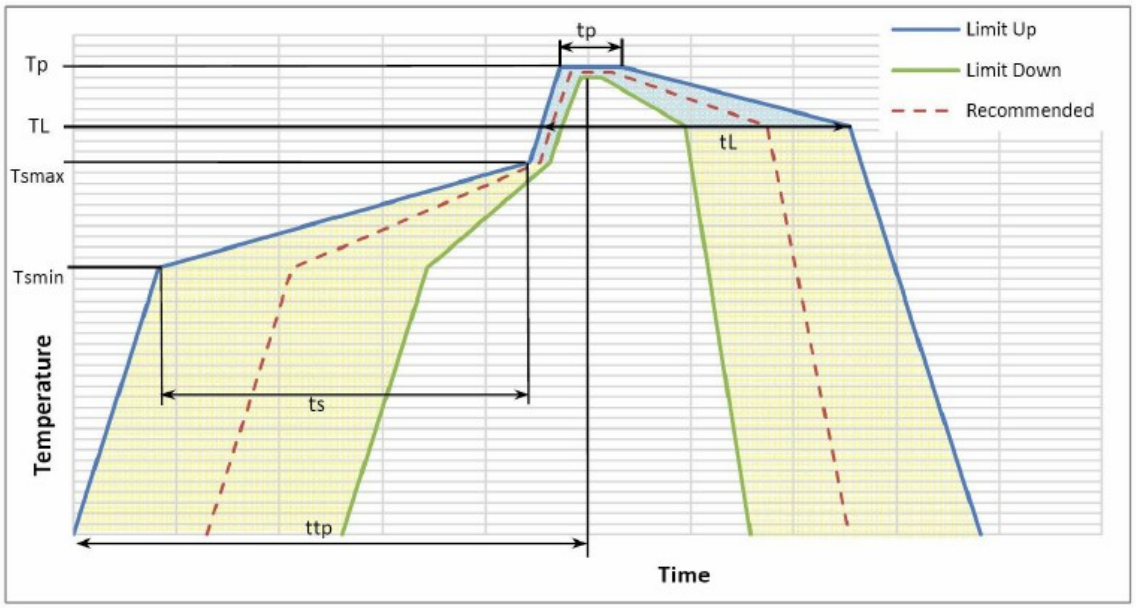
13.7. Solder Paste

	Lead free
Solder Paste	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

13.7.1. Solder Reflow

The following is the recommended solder reflow profile:



Profile Feature	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3℃/second max
Preheat **- Temperature Min (Tsmin)** **- Temperature Max (Tsmax)** **- Time (min to max) (ts)**	 150℃ 200℃ 60 ~ 180 seconds
Tsmax to TL **- Ramp-up Rate**	 3℃/second max
Time maintained above: **- Temperature (TL)** **- Time (tL)**	 217℃ 60 ~150 seconds

Profile Feature	Pb-Free Assembly
Peak Temperature (T_P)	245 +0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10 ~30 seconds
Ramp-down Rate	6 ℃/sec max
Time 25℃ to Peak Temperature	8 minutes max

NOTE:

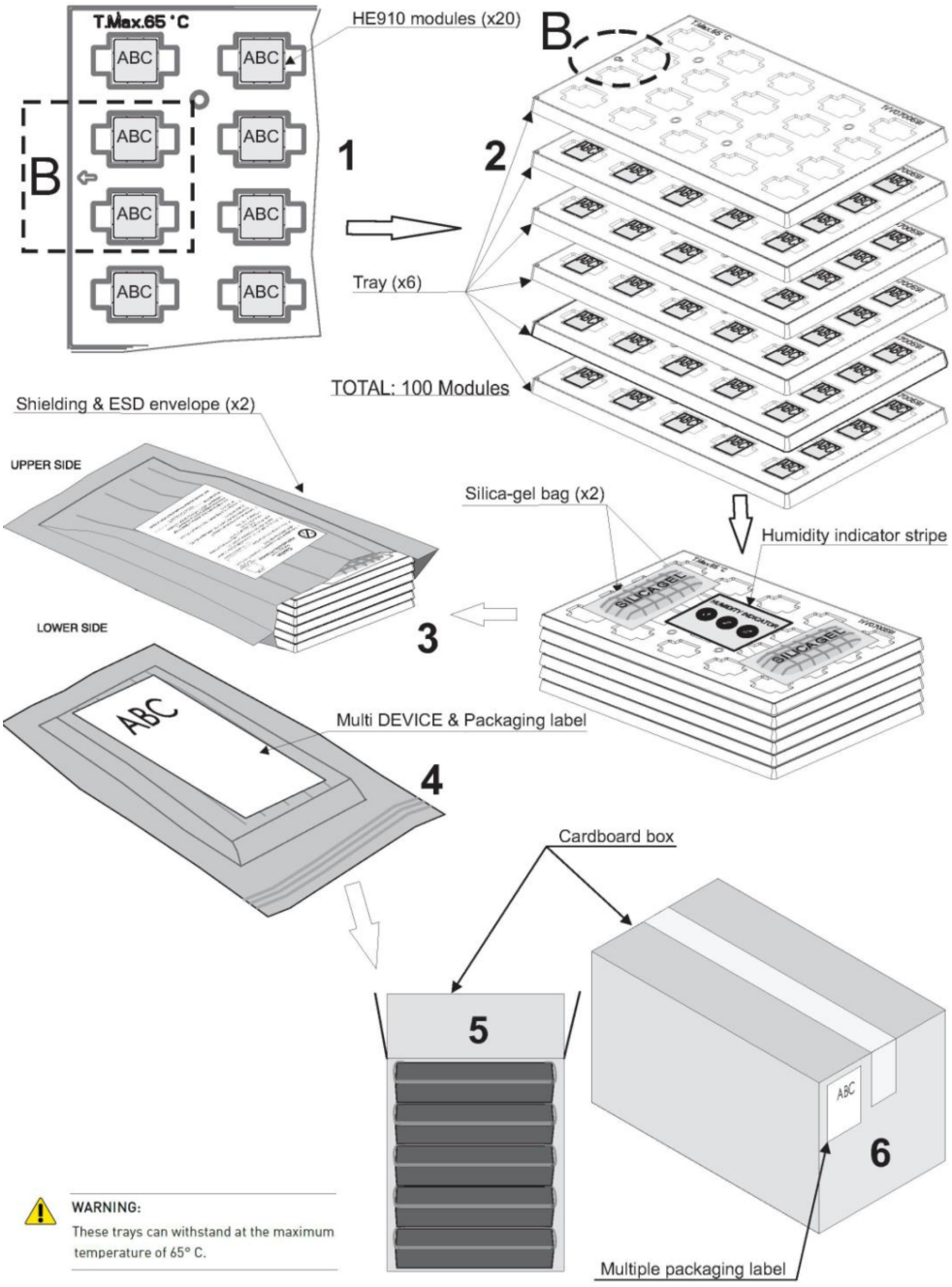
All temperatures refer to topside of the package, measured on the package body surface.

WARNING:

The CE910-SL module withstands one reflow process only.

14. Packing System

The CE910-SL modules are packaged on trays of 20 pieces each. These trays can be used in SMT processes for pick & place handling.



14.1. Moisture Sensibility

The CE910-SL is a Moisture Sensitive Device level 3, in accordance with standard IPC/JEDEC J-STD-020, take care all the relative requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at < 40°C and 90% relative humidity (RH).

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168hours if condition b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more

15. Application Design Guide

15.1. Download and Debug Port

One of the following options should be chosen in the design of host system in order to download or upgrade the Telit's software and debug CE910-SL when CE910-SL is already mounted on a host system.

CASE I:
Users who use both of UART and USB interfaces to communicate with CE910-SL

- Must implement a download method in a host system for upgrading CE910-SL when it's mounted.

CASE II:
Users who use USB interface only to communicate with CE910-SL

- Must arrange UART port in a host system for debugging or upgrading CE910-SL when it's mounted.

CASE III:

Users who use UART interface only to communicate with CE910-SL

- Must arrange USB port in a host system for debugging or upgrading CE910-SL when it's mounted.

16. Safety Recommendations

READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country's regulations and the specific environmental regulation.

Do not disassemble the product; any evidence of tampering will compromise the warranty validity. Follow the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to conform to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pads because electrostatic discharges may damage the product itself.
The system integrator is responsible for the functioning of the final product; therefore, care has to be taken with the external components of the module as well as of any project or installation issue because of the risk of disturbing the CDMA network or external devices or having impact on security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against SAR regulations.

17. Document History

Revision	Date	Changes
0	2014-11-19	Initial release for MKT sample
1	2015-03-12	Updated 2.2 Thickness 2.35mm Removed section 8 Modem Serial port 2 Removed 8.2 Modem serial port 2 Updated 13.2 Module finishing & Dimension: Thickness 2.35mm Updated Module layout dimension Removed Section 16 Conformity Assessment Issues
2	2015-12-02	Updated 1.4 Document Organization, section 9 Updated 1.6: Related Document Updated 2.2 Product Specifications Weight 3.6 gram Delete “Reserved” mark. 3.1 Digital Voice Interface Updated 5.2 Power Consumptions, Update Current and Removed “TBD” Added section 9 Audio section overview Updated section 13.2 “ Module Finishing & Dimensions” Updated 13.2 Module Weight 3.6 g Removed 13.2 Module finishing & Dimension: Planarity
3	2016-05-04	Added section 2.3 Operating Frequency Updated 4.4 Hardware unconditional Shutdown