CL865 Hardware User Guide

1vv0301104 Rev.2 – 2015-05-22

Making machines talk.

APPLICABILITY TABLE

PRODUCT
CL865-DUAL
CL865-SC

SPECIFICATIONS SUBJECT TO CHANGE WITHOUT NOTICE

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Contents

1. Introduction

1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit CL865 module.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our CL865 modules.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "General Product Description" gives an overview of the features of the product.

Chapter 3: "CL865 Mechanical Dimensions"

Chapter 4: "CL865 Module Connections" deals with the pin out configuration and layout.

Chapter 5: "Hardware Commands" How to operate on the module via hardware.

Chapter 6: "Power supply" Power supply requirements and general design rules.

Chapter 7: "Antenna" The antenna connection and board layout design are the most important parts in the full product design.

Chapter 8: "USB ports" The USB port on the Telit CL865 is the core of the interface between the module and OEM hardware

Chapter 9: "Serial ports" The serial port on the Telit CL865 is the core of the interface between the module and OEM hardware

Chapter 10: "Audio Section overview"

Chapter 11: "General Purpose I/O" How the general purpose I/O pads can be configured.

Chapter 12 "DAC and ADC Section" Deals with these two kind of converters.

Chapter 13: "Mounting the CL865 on your board" Recommendations and specifics on how to mount the module on the user's board.

Chapter 14: "Packaging system" Recommendations and specifics on how the system is packaged.

Chapter 15: "Application Design Guide" Deals with the design of host system for download or upgrade.

Chapter 16: "Certifications and Conformity"

Chapter 17: "Safety Recommendations"

Chapter 18: "Document History" Holds all document changes

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- CL865 Software User Guide, 1vv0301105
- Audio settings application note , 80000NT10007a
- CL865 AT Commands Reference Guide, 80428ST10592A
- Telit EVK2 User Guide, 1vv0300704

2. General Product Description

2.1. Overview

The aim of this document is the description of typical hardware solutions useful for developing a product with the Telit CL865 module.

In this document all the basic functions of a mobile device will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace all hardware solutions and products that may be designed. Avoiding the discussed wrong solutions must be considered as mandatory. While the suggested hardware configurations must not be considered mandatory, the information given must be used as a guide and a starting point for properly developing a product with the Telit CL865 module.

NOTE:

The integration of the CDMA 1xRTT module within a user application must be done according to the design rules described in this manual.

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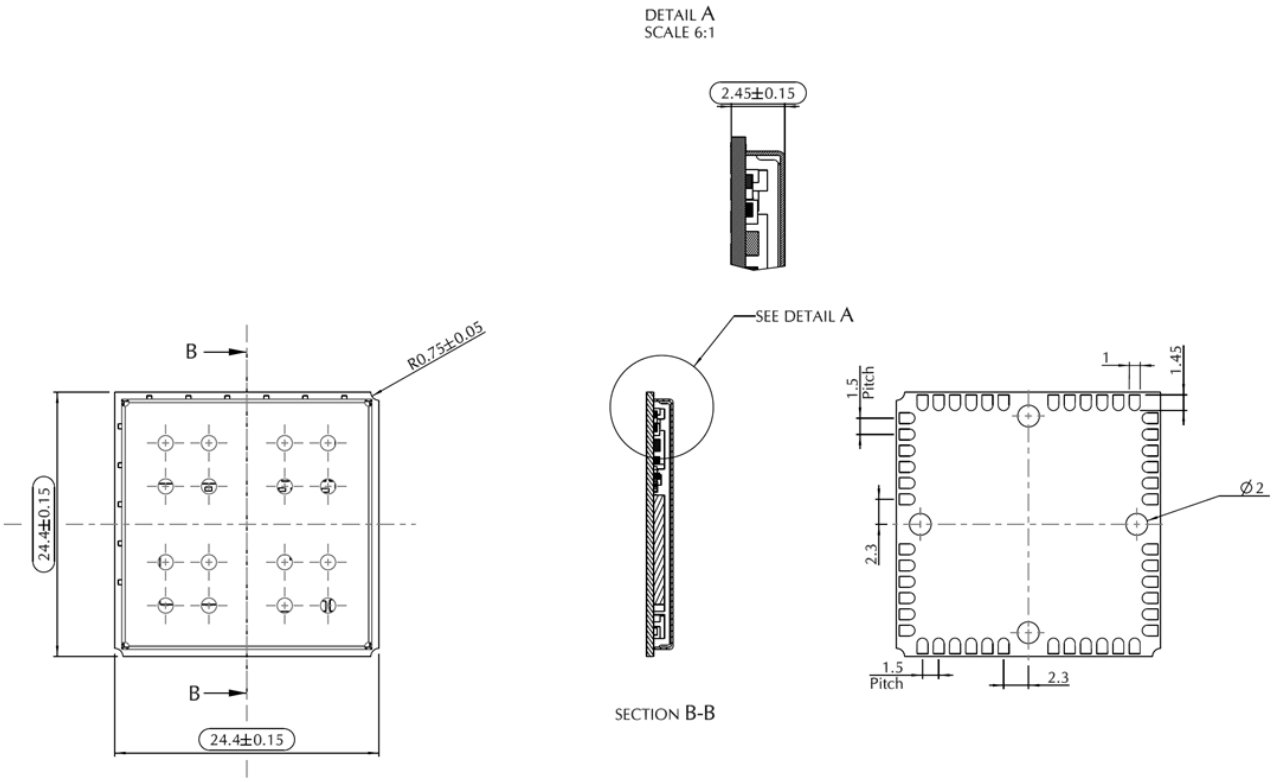
2.2. Product Specifications

CL865 Specifications	
Air Interface	CDMA 1xRTT
Frequency Bands	CL865-DUAL : 800/1900MHz (BC0/BC10/BC1) CL865-SC : 800MHz(BC0)
Data Service	CDMA 1xRTT: 153.6 Kbps (full-duplex)
Max. RF out power	• CDMA BC0: Power class 3 (24.5dBm) for 1xRTT • CDMA BC10 subclass2,3: Power class 2 (24.5dBm) for 1xRTT • CDMA BC1: Power class 2 (24.5dBm) for 1xRTT
Typical conducted sensitivity	• CDMA BC0: –108dBm • CDMA BC10: –108dBm • CDMA BC1: –107dBm
Device dimensions	24.4mm(L) x 24.4mm(W) x 2.45mm(T)
Weight	3.0g
Storage and Operating Temperature Range	–40 ~ +85°C
Normal operating voltage range	3.4 ~ 4.2V
IO voltage	1.8V
Interface	• 48 Very Thin Quad Flat Non-Leaded Package(VQFN) interface • 8 general I/O ports maximum including multi-functional I/Os • State LED output • 2 A/D converter • 1 D/A converter • Full RS232 CMOS UART: baud rate up to 4Mbps • Reserved two wires CMOS UART for debugging • USB 2.0: baud rate up to 12Mbps
Antenna	Primary antenna, 800/1900MHz (BC0/BC10/BC1)
Audio	Analog audio interface (1 EAR/MIC)
Message	SMS (MO/MT)
Approvals	CL865-DUAL: • Regulatory : FCC, IC • Carrier: Verizon, Sprint CL865-SC: • Regulatory : CCC, SRRC

3. CL865 Mechanical Dimensions

The CL865 overall dimensions are:

Length:	24.4 mm
Width:	24.4 mm
Thickness:	2.45 mm
Weight	3 g



4. CL865 module connections

4.1. PIN-OUT

Pad	Signal	I/O	Function	Note	Type
USB					
18	USB_D+	I/O	USB differential Data (+)		
17	USB_D-	I/O	USB differential Data (-)		
16	USB_VBUS	AI	Power for the internal USB transceiver.		5V
RUIM card interface(*NOTE)					
9	RUIMVCC	-	Reserved but applicable only to RUIM variant : Power supply for the RUIM		1,8 / 3V
10	RUIMRST	O	Reserved but applicable only to RUIM variant : RUIM Reset		1,8 / 3V
11	RUIMCLK	O	Reserved but applicable only to RUIM variant : RUIM Clock		1,8 / 3V
12	RUIMIO	I/O	Reserved but applicable only to RUIM variant : RUIM Data I/O		1,8 / 3V
X All GPI0 can be program med	RUIMIN	I	Reserved but applicable only to RUIM variant : RUIM IN		CMOS 1.8V
Auxiliary UART					
44	RXD_AUX	I	Auxiliary UART (RX Data from DTE)		CMOS 1.8V
45	TXD_AUX	O	Auxiliary UART (TX Data to DTE)		CMOS 1.8V
Prog. / Data + HW Flow Control					
1	C109/DCD/GPO	O	Output for Data carrier detect signal (DCD) to DTE / GP output		CMOS 1.8V
2	C125/RING/GPO	O	Output for Ring indicator signal (RI) to DTE / GP output		CMOS 1.8V
3	C107/DSR/GPO	O	Output for Data set ready signal (DSR) to DTE / GP output		CMOS 1.8V
4	C108/DTR/GPI	I	Input for Data terminal ready signal (DTR) from DTE / GP input		CMOS 1.8V
5	C105/RTS/GPI	I	Input for Request to send signal (RTS) from DTE / GP input		CMOS 1.8V
6	C106/CTS/GPO	O	Output for Clear to send signal (CTS) to DTE / GP output		CMOS 1.8V
7	C103/TXD	I	Serial data input (TXD) from DTE		CMOS 1.8V
8	C104/RXD	O	Serial data output to DTE		CMOS 1.8V
DAC and ADC					
13	ADC_IN1	AI	Analog/Digital converter input		A/D
14	ADC_IN2	AI	Analog/Digital converter input		A/D
15	DAC_OUT	AO	Digital/Analog converter output		D/A
Miscellaneous Functions					
30	VRTC	I	RTC power		Power
47	RESET*	I	Hardware Unconditional Restart		Pull up to VBATT
43	V_AUX / PWRMON	O	1.8V stabilized output Imax=100mA		Power Out 1.8V

Pad	Signal	I/O	Function	Note	Type
			/ Power ON monitor		
34	Antenna	I/O	Antenna pad – 50 Ω		RF
GPIO					
42	GPIO_01 / DVI_WA0	I/O	GPIO01 Configurable GPIO / Digital Audio Interface (WA0)		CMOS 1.8V
41	GPIO_02 / DVI_RX	I/O	GPIO02 Configurable GPIO / Digital Audio Interface (RX)		CMOS 1.8V
40	GPIO_03 / DVI_TX	I/O	GPIO03 Configurable GPIO / Digital Audio Interface (TX)		CMOS 1.8V
39	GPIO_04 / DVI_CLK	I/O	GPIO04 Configurable GPIO / Digital Audio Interface (CLK)		CMOS 1.8V
29	GPIO_05	I/O	GPIO05 Configurable GPIO		CMOS 1.8V
28	GPIO_06 / ALARM	I/O	GPIO06 Configurable GPIO / ALARM		CMOS 1.8V
27	GPIO_07	I/O	GPIO07 Configurable GPIO		CMOS 1.8V
26	GPIO_08 / STAT_LED	I/O	GPIO08 Configurable GPIO / STAT_LED		CMOS 1.8V
Analog Voice Interface					
21	EAR+	AO	Earphone signal output, phase +		
20	EAR-	AO	Earphone signal output, phase -		
24	MIC+	AI	Microphone input, phase +		
22	MIC-	AI	Microphone input, phase -		
Power Supply					
38	VBATT	-	Main power supply (Baseband)		Power
37	VBATT_PA	-	Main power supply (Radio PA)		Power
23	AGND	-	AF Signal Ground (see audio section)		AF Signal
32	GND	-	Ground		Power
33	GND	-	Ground		Power
35	GND	-	Ground		Power
36	GND	-	Ground		Power
46	GND	-	Ground		Power
23	GND	-	Ground		-
RESERVED					
19		-			
25		-			
31					
48		-			

NOTE:

RUIM interface is reserved for Verizon/Sprint variants and it is applicable only to RUIM variants of CL865 (CL865-SC)

WARNING:

Reserved pins must not be connected.

NOTE:

The following table is listing the main Pinout differences between the CL865 variants.

Product	BC0	BC10	BC1	Notes
CL865-DUAL	Yes	Yes	Yes	Reserved pads : 9, 10, 11, 12
CL865-SC	Yes	No	No	

NOTE:

If not used, almost all pins should be left disconnected. The only exceptions are the following pins:

Pad	signal	
38, 37	VBATT & VBATT_PA	
32, 33, 35, 36, 46	GND	
23	AGND	
7	C103/TXD	If not used should be connected to a Test Point
8	C104/RXD	If not used should be connected to a Test Point
5	C105/RTS	If not used should be connected to a Test Point
6	C106/CTS	If not used should be connected to a Test Point
43	V_AUX / PWRMON	
47	RESET*	
45	TXD_AUX	If not used should be connected to a Test Point
44	RXD_AUX	If not used should be connected to a Test Point
18	USB D+	If not used should be connected to a Test Point or an USB connector
17	USB D-	If not used should be connected to a Test Point or an USB connector
16	USB_VBUS	If not used should be connected to a Test Point or an USB connector

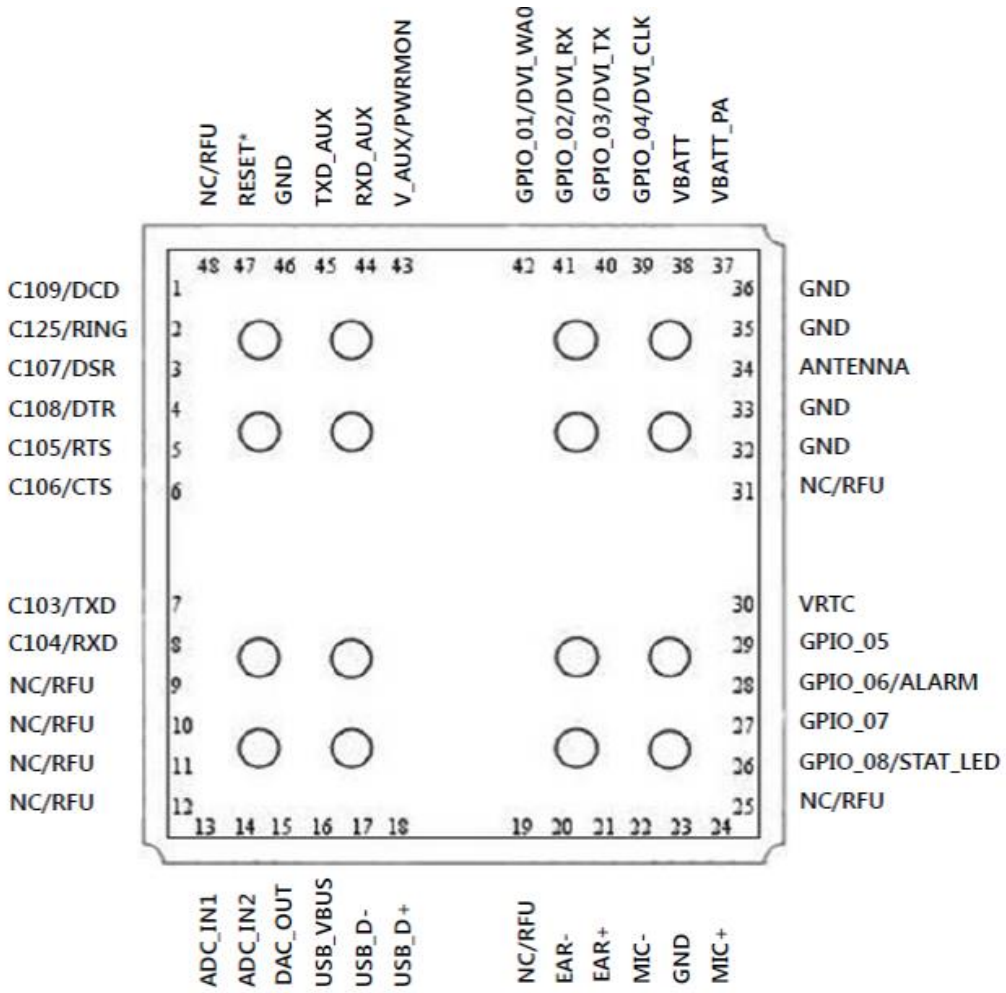
NOTE:

RTS must be connected to the GND (on the module side) if flow control is not used

4.2. PIN Layout

4.2.1.VQFN Pads Layout(CL865-DUAL)

TOP VIEW

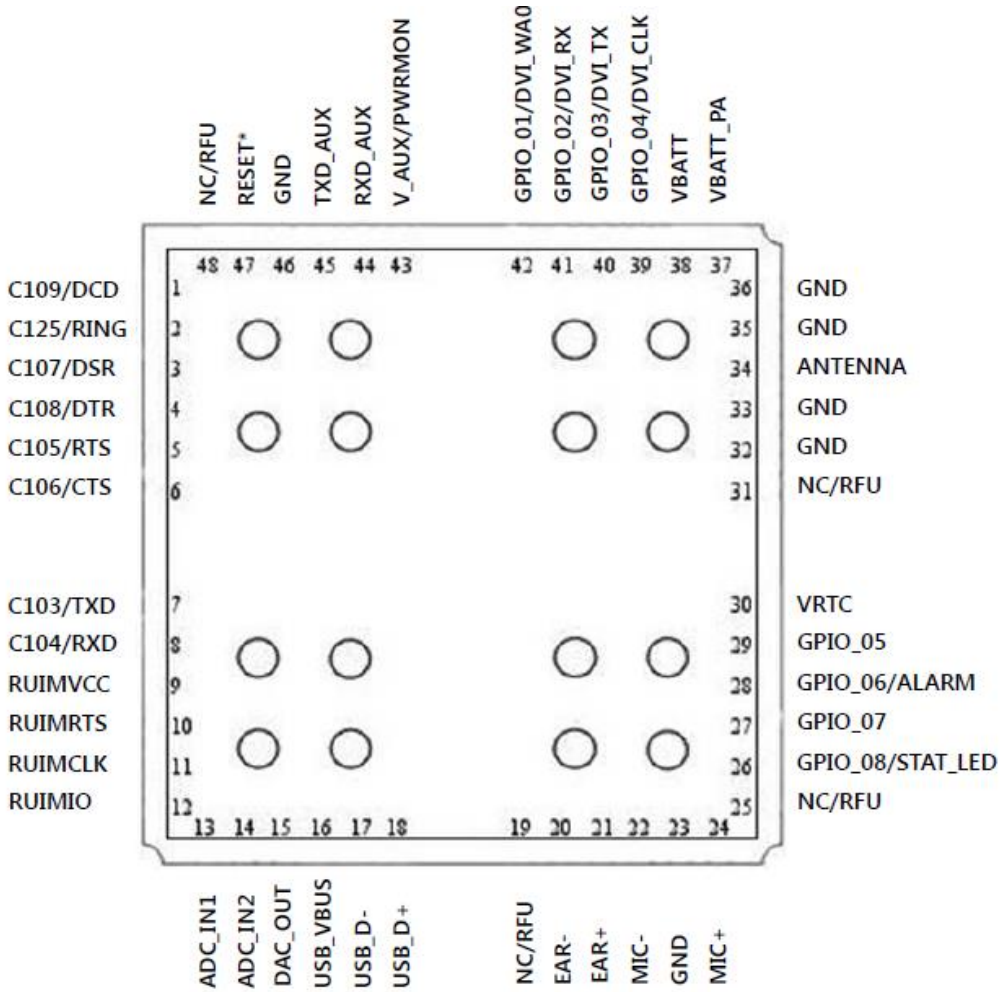


NOTE:

The pins defined as NC/RFU shall be considered RESERVED and must not be connected to any pin in the application.

4.2.2.VQFN Pads Layout(CL865-SC)

TOP VIEW



NOTE:

The pins defined as NC/RFU shall be considered RESERVED and must not be connected to any pin in the application.

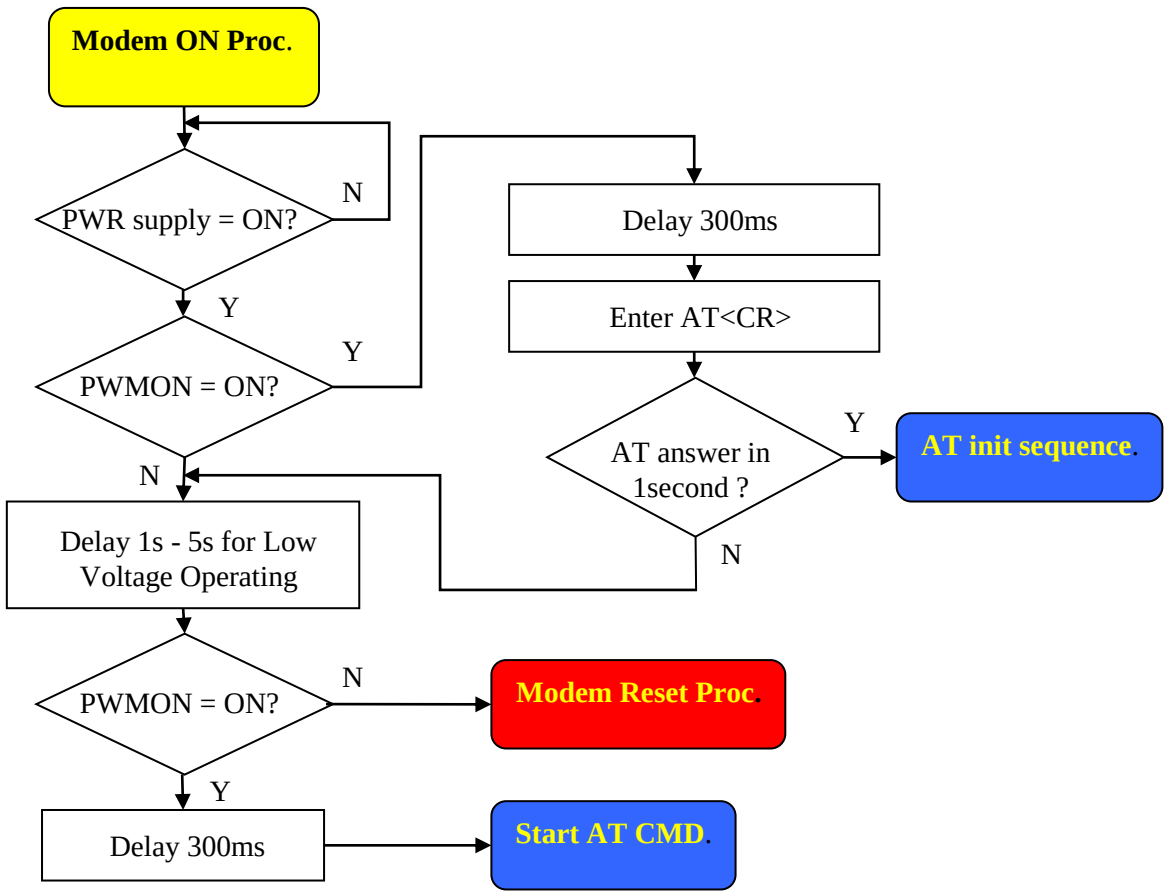
5. Hardware Commands

5.1. Auto-Turning ON the CL865

The CL865 will automatically power on itself when VBATT & VBATT_PA are applied to the module.

V_AUX / PWRMON pin will be at the high logic level and the module can be considered fully operating after 5 seconds.

The following flow chart shows the proper turn on procedure:



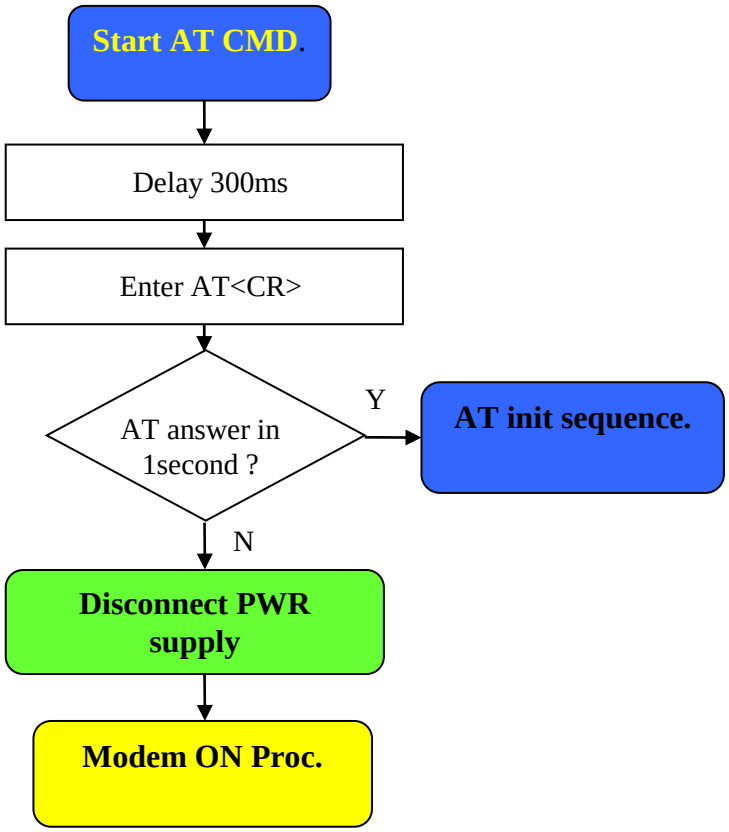
NOTE:

The power supply must be applied either at the same time on pins VBATT and VBATT_PA.

NOTE:

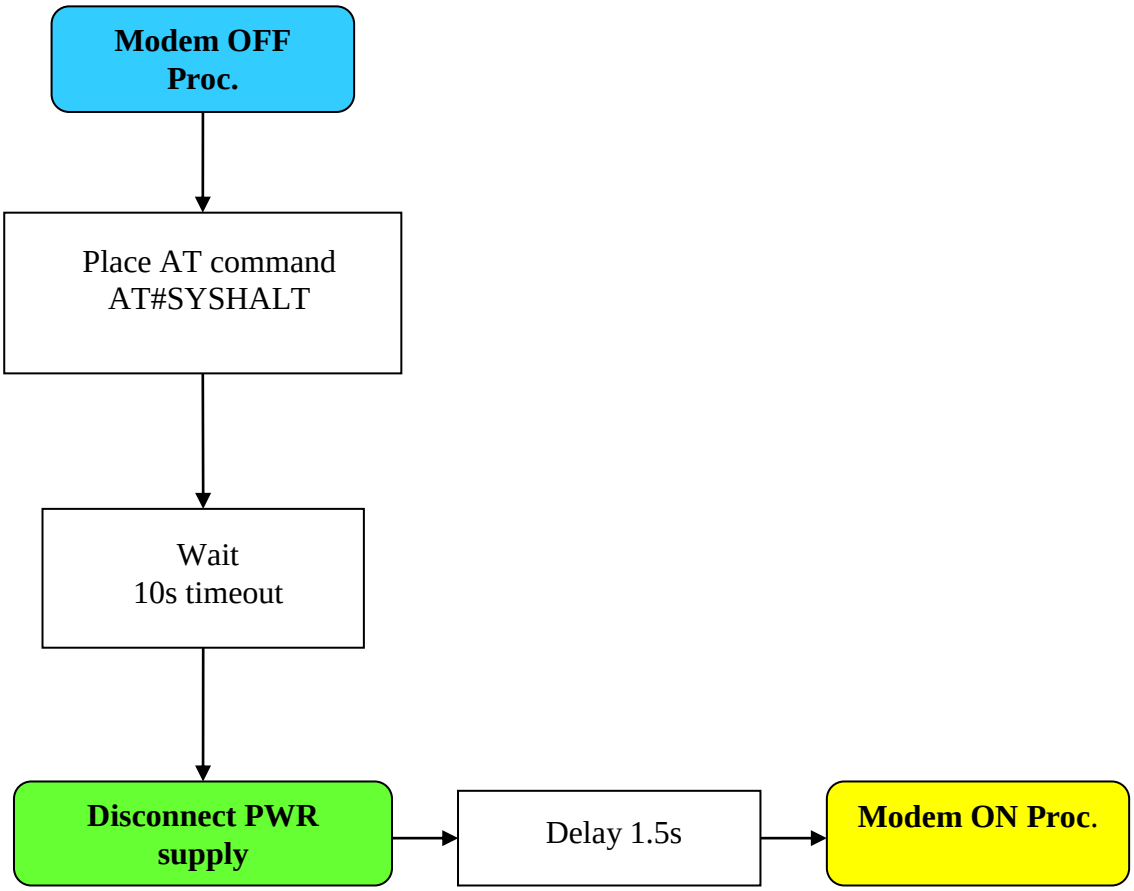
In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CL865 when the module is powered OFF or during an ON/OFF transition.

A flow chart showing the AT commands managing procedure is displayed below:



5.2. Turning OFF the CL865

The following flow chart shows the proper turnoff procedure:



NOTE:

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CL865 when the module is powered OFF or during an ON/OFF transition.

5.3. Resetting the CL865

5.3.1. Hardware Unconditional restart

To unconditionally reboot the CL865, the pad RESET* must be tied low for at least 200 milliseconds and then released.

WARNING:

The hardware unconditional Restart must not be used during normal operation of the device since it does not detach the device from the network. It shall be kept as an emergency exit procedure to be done in the rare case that the device gets stuck waiting for some network or RUIM responses.

NOTE:

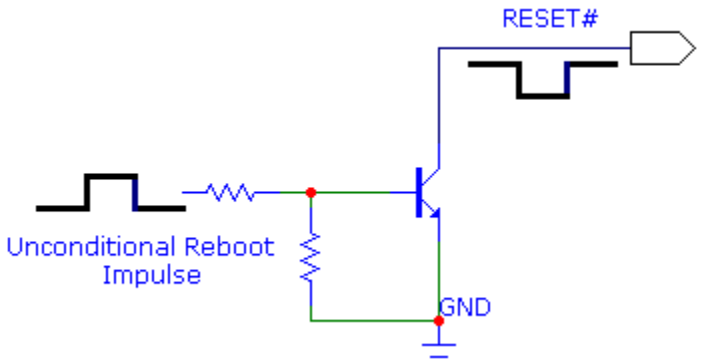
Do not use any pull up resistor on the RESET* line nor any totem pole digital output. Using pull up resistor may bring to latch up problems on the UL865 power regulator and improper functioning of the module.

The line RESET* must be connected only in open collector configuration; the transistor must be connected as close as possible to the RESET* pin.

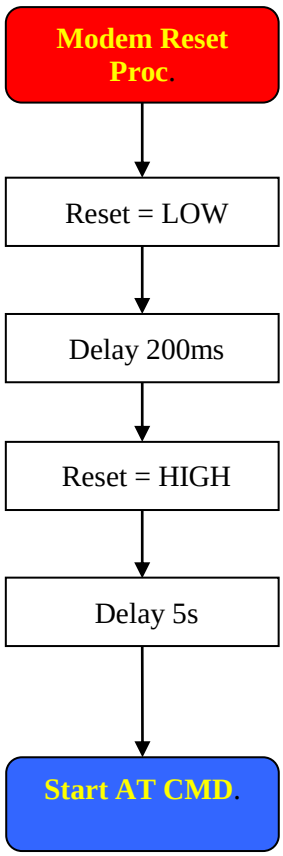
TIP:

The unconditional hardware restart must always be implemented on the boards and the software must use it as an emergency exit procedure.

A simple circuit to do it is:



In the following flow chart is detailed the proper restart procedure:



NOTE:

In order to prevent a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CL865 when the module is powered OFF or during an ON/OFF transition.

6. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product overall performance, hence read the requirements carefully and the guidelines that will follow for a proper design.

6.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT_PA signals and must fulfill the following requirements:

POWER SUPPLY	
Nominal Supply Voltage	3.8 V
Normal Operating Voltage Range	3.4 V ~ 4.2 V
Extended Operating Voltage Range	3.4 V ~ 4.5 V

NOTE:

The Operating Voltage Range MUST never be exceeded. Special care must be taken when designing the application's power supply section to avoid having an excessive voltage drop.

If the voltage drop is exceeding the limits it could cause a Power Off of the module.

Behavior in the extended operating voltage range might deviate from 3GPP2 specification.

WARNING:

The Sudden power loss is never allowed during the modem normal operation.
If interruption the program and erase operation through sudden power loss,
They could be a cause of the device gets stuck.

6.2. Power Consumption

Current Consumption		
Mode	**Average (mA)**	**Mode Description**
Power off current (Typical)		140uA(*1)
Standby mode		No call in progress (slot cycle index=2)
AT+CFUN=1	31	Normal mode; full functionality of the module
AT+CFUN=4	28	Disabled TX and RX; modules is not registered on the network
AT+CFUN=5	1.5 (*2)	CFUN=5 full functionality with power saving; Module registered on the network can receive incoming calls and SMS
Tx and Rx mode		A call in progress
Max Power Mode	680	CDMA 1x voice/data call

(*1)The off current is the total supply current from the main battery with the XO regulator ON, 19.2MHz XO ON and others are OFF.
(*2) Standby current consumption depends on network configuration or module configuration. The current consumption value for CFUN=5 is measured under slot cycle index=2.

TIP:

The electrical design for the power supply should be made ensuring it will be capable of a peak current output of at least 1A.

6.3. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout

6.3.1. Electrical Design Guidelines

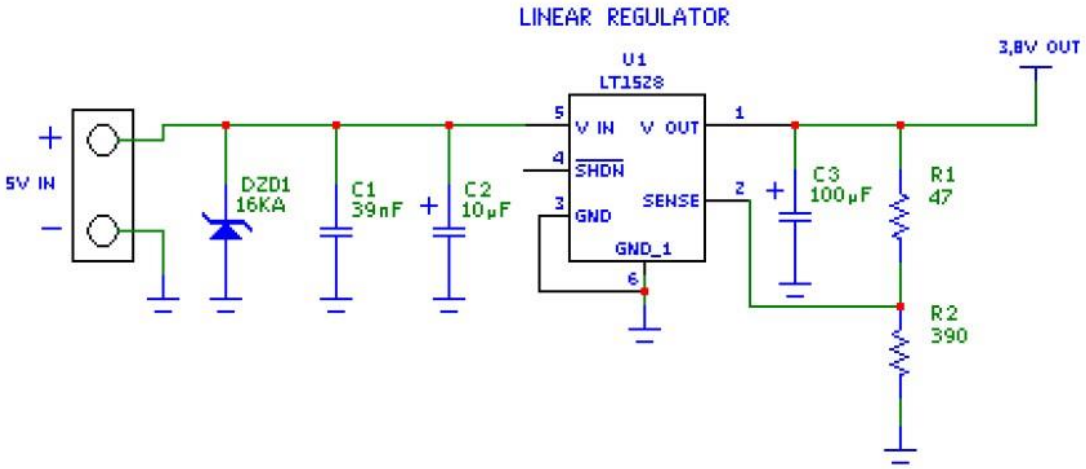
The electrical design of the power supply depends strongly on the power source from which this power is drained. We will distinguish them into three categories:

- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

6.3.2.+ 5V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there is not a big difference between the input source and the desired output so a linear regulator can be used. A switching power supply will not be suitable because of the low drop-out requirements.
- When using a linear regulator, a proper heat sink must be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the CL865. A 100µF tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the power input in order to save the CL865 from power polarity inversion.

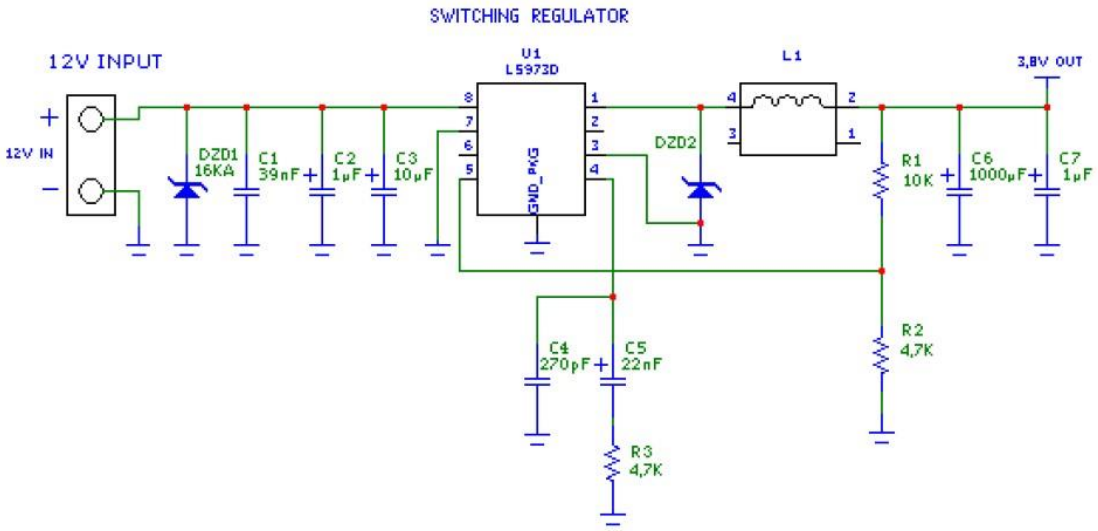
An example of linear regulator with 5V input is:



6.3.3.+ 12V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suitable and must not be used. A switching power supply would be preferable because of its better efficiency, especially with the 1A peak current load represented by CL865.
- When using a switching regulator, a 500 kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case, the frequency and switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15.8V and this must be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks. A 100µF tantalum capacitor is usually suited for this.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For car applications a spike protection diode must be inserted close to the power input in order to clean the supply from spikes.
- A protection diode must be inserted close to the power input in order to save the CL865 from power polarity inversion. This can be the same diode as for spike protection.

An example of switching regulator with 12V input is in the below schematic:



6.3.4. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V. A single 3.7V lithium-ion cell battery type is ideal to supply power to the Telit CL865 module.

WARNING:

The three cells Ni/Cd or Ni/MH 3.6 V Nom. battery types or 4V PB types ***MUST NOT BE USED DIRECTLY*** since their maximum voltage can rise over the absolute maximum voltage for the CL865 and damage it.

NOTE:

DON'T USE any Ni-Cd, Ni-MH, and Pb battery types directly connected with CL865. Their use can lead to overvoltage on the CL865 and damage it. USE ONLY Li-Ion battery types.

- A bypass low (usually a 100uF tantalum) ESR capacitor with adequate capacity must be provided in order to cut the current absorption peaks.
- Make sure the low ESR capacitor (usually a tantalum) is rated at least 10V.
- A protection diode must be inserted close to the power input in order to protect the CL865 module from power polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 1A. The suggested battery capacity is from 500mAh to 1000mAh.

6.3.5. Thermal Design Guidelines

The thermal design for the power supply heat sink must be done with the following specifications:

- Average current consumption during CDMA 1x @PWR level max : 680mA

NOTE:

The average consumption during transmissions depends on the power level at which the device is requested to transmit via the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

If we assume that the device stays in transmission for short periods of time (a few minutes) and then remains for quite a long time in idle (one hour), then the power supply always has time to cool down between the calls and the heat sink could be smaller than the calculated for 680mA maximum RMS current. There could even be a simple chip package (no heat sink).

Moreover in average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than 680 mA (usually around 300 mA).

For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.

The heat generated by the CL865 must be taken into consideration during transmission at 24.5dBm max during calls. This generated heat will be mostly conducted to the ground plane under the CL865. The application must be able to dissipate heat.

In the CDMA 1x mode, since CL865 emits RF signals continuously during transmission, special attention must be paid to how to dissipate the heat generated.

The current consumption will be up to about 680mA in CDMA 1x continuously at the maximum TX output power (24.5dBm). Thus, you must arrange the area on the application PCB must be as large as possible under CL865.

The CL865 must be mounted on the large ground area of the application board and make many ground vias to dissipate the heat.

6.3.6. Power Supply PCB layout Guidelines

As seen in the electrical design guidelines, the power supply must have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct operation of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

- The bypass low ESR capacitor must be placed close to the Telit CL865 power input pads, or if the power supply is a switching type, the capacitor can be placed close to the inductor to cut the ripple if the PCB trace from the capacitor to CL865 is wide enough to ensure a drop-less connection even during the 1A current peaks.
- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 1A current peaks are absorbed. While a voltage drop of hundreds of mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If the application does not have an audio interface but only uses the data feature of the Telit CL865, then this noise is not as disruptive and the power supply layout design can be more forgiving.
- The PCB traces to CL865 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 1A current peaks are absorbed. This is a must for the same above-mentioned reasons. Try to keep this trace as short as possible.
- The PCB traces connecting the switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (usually 100-500 kHz).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board must be done in a way to guarantee that the high current return paths in the ground plane are not overlapped with any noise sensitive circuitry such as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables must be kept separate from noise sensitive lines such as microphone/earphone cables.

7. Antenna

The antenna connection and board layout design are the most important parts in the full product design and they strongly reflect on the product's overall performance. Read carefully and follow the requirements and the guidelines for a proper design.

7.1. CDMA Antenna Requirements

The antenna for a Telit CL865 device must fulfill the following requirements:

CL865 Specifications	
Frequency range	Depending on the frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s)
Bandwidth	70 MHz in CDMA BC0 53 MHz in CDMA BC10 (subclass 2,3) 140 MHz in CDMA BC1
Gain	Gain < 5.12dBi in CDMA BC0 Gain < 5.12dBi in CDMA BC10 (subclass 2,3) Gain < 6.12dBi in CDMA BC1
Impedance	50 Ohm
Input power	> 24.5dBm Average Power in CDMA
VSWR absolute max	≤ 5:1 (Limit to avoid permanent damage)
VSWR recommended	≤ 2:1 (Limit to fulfill all regulatory requirement)

Furthermore if the device is developed for the US and/or Canada market, it must comply with the FCC and/or IC approval requirements:

This device is to be used only for mobile and fixed application. The antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all persons and must not be co-located or operating in conjunction with any other antenna or transmitter. End-Users must be provided with transmitter operation conditions for satisfying RF exposure compliance. OEM integrators must ensure that the end user has no manual instructions to remove or install the CL865 module. Antennas used for this OEM module must not exceed 5dBi gain for mobile and fixed operating configurations.

7.1.1.CL865 Antenna – PCB line Guidelines

When using the Telit CL865 module, since there's no antenna connector on the module, the antenna must be connected to the CL865 through the PCB with the antenna pad (**pin 34**).

In the case that the antenna is not directly developed on the same PCB, hence directly connected at the antenna pad of the CL865, then a PCB line is needed in order to connect with it or with its connector.
This transmission line shall fulfill the following requirements:

ANTENNA LINE ON PCB REQUIREMENTS	
Impedance	50 ohm
Max Attenuation	0.3 dB
No coupling with other signals allowed	
Cold End (Ground Plane) of antenna shall be equipotential to the CL865 ground pins	

This transmission line should be designed according to the following guidelines:

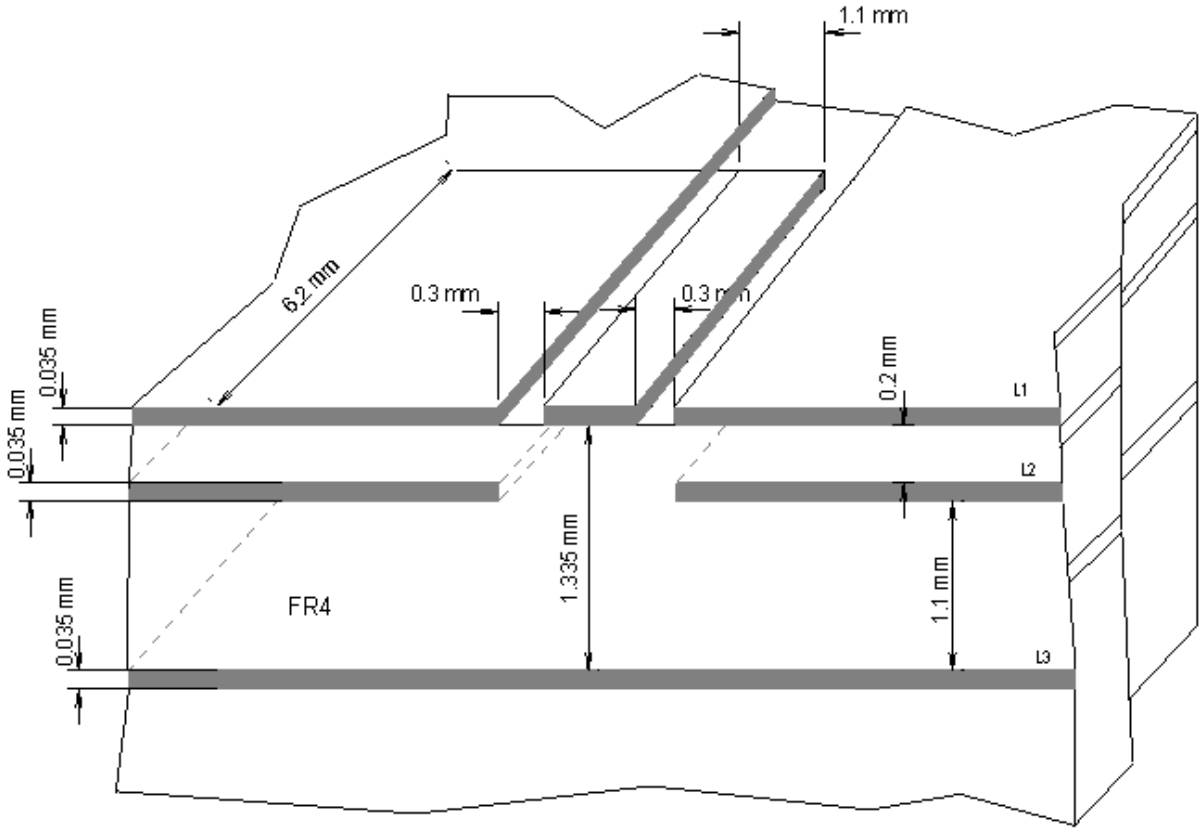
Ensure that the antenna line impedance is 50 ohm;
Keep the antenna line on the PCB as short as possible, since the antenna line loss shall be less than 0.3 dB;
Antenna line must have uniform characteristics, constant cross section; avoid meanders and abrupt curves;
Keep, if possible, one layer of the PCB used only for the Ground plane;
Surround (on the sides, over and under) the antenna line on PCB with Ground, avoid having other signal tracks facing directly the antenna line track;
The ground around the antenna line on PCB has to be strictly connected to the Ground Plane by placing vias every 2mm at least;
Place EM noisy devices as far as possible from CL865 antenna line;
Keep the antenna line far away from the CL865 power supply lines;
If you have EM noisy devices around the PCB hosting the CL865, such as fast switching ICs, take care of the shielding of the antenna line by burying it inside the layers of PCB and surround it with Ground planes, or shield it with a metal frame cover.
If you don't have EM noisy devices around the PCB of CL865, by using a micro strip on the superficial copper layer for the antenna line, the line attenuation will be lower than a buried one;

7.2. PCB Guidelines in case of FCC certification

In the case FCC certification is required for an application using CL865, according to FCC KDB 996369 for modular approval requirements, the transmission line has to be similar to that implemented on CL865 interface board and described in the following chapter.

7.2.1. Transmission line design

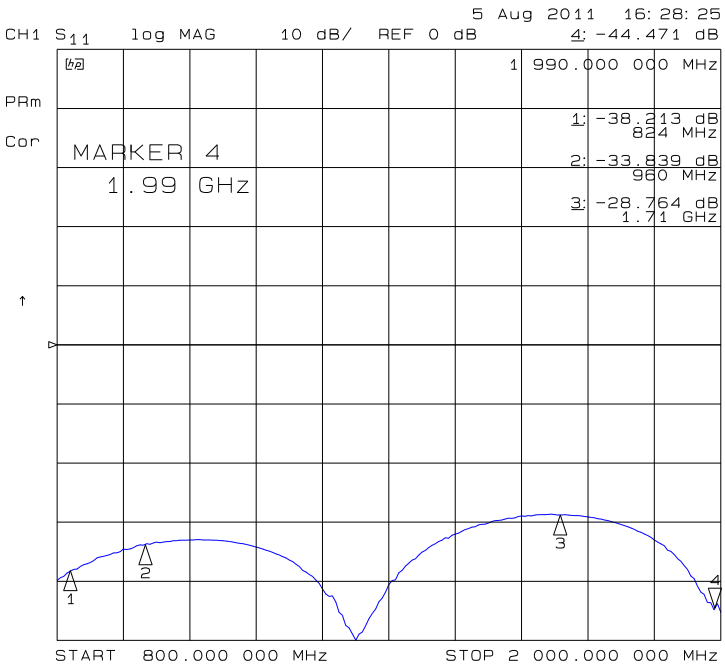
During the design of the CL865 interface board, the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.
The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity ε_r = 4.6 ± 0.4 @ 1 GHz, TanD= 0.019 ÷ 0.026 @ 1 GHz.
A characteristic impedance of nearly 50 Ω is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is 51.6 Ω, estimated line loss is less than 0.1 dB. The line geometry is shown below:



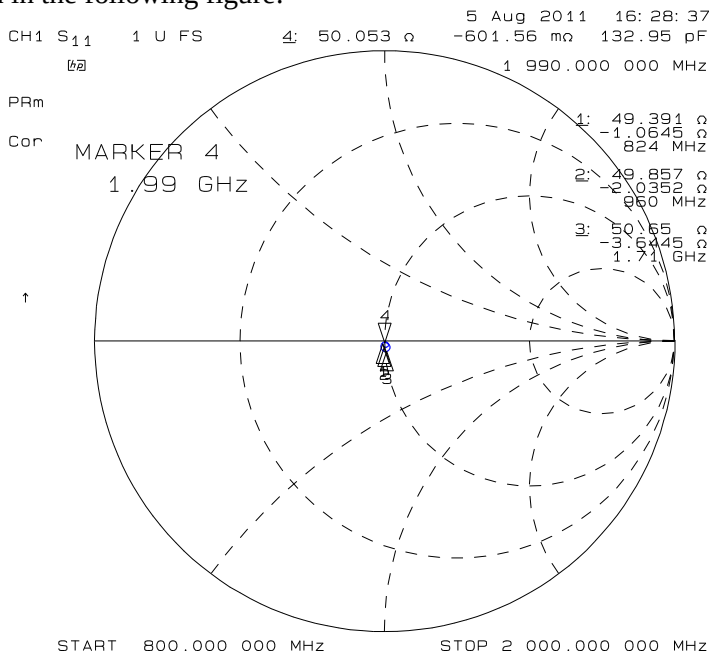
7.2.2.Transmission line measurements

HP8753E VNA (Full-2-port calibration) has been used in this measurement session. A calibrated coaxial cable has been soldered at the pad corresponding to CL865 RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50 Ω load.

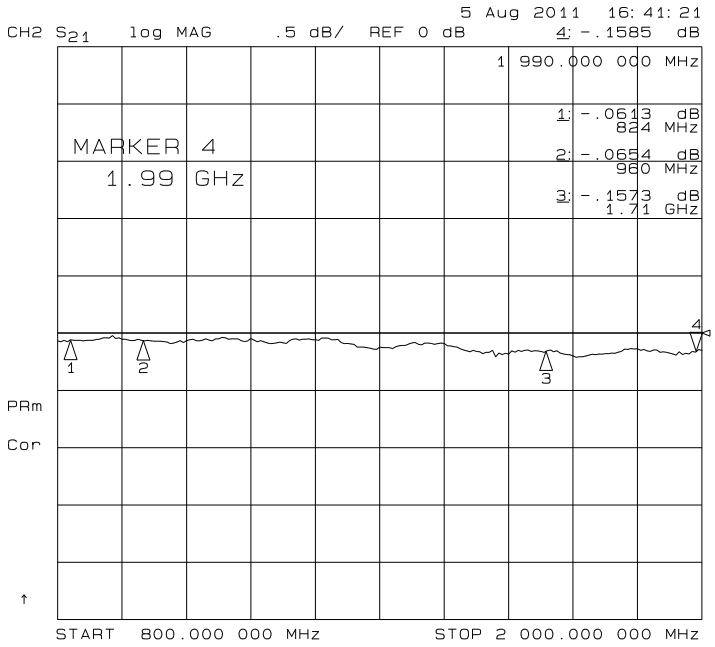
Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50 Ω load) is shown in the following figure:



Insertion Loss of G-CPW line plus SMA connector is shown below:



7.3. Antenna - Installation Guidelines

- Install the antenna in a place covered by the CDMA signal.
- If the device antenna in the application is located greater than 20cm from the human body and there are no co-located transmitters then the Telit FCC/IC approvals can be re-used by the end product.
- Antenna shall not be installed inside metal cases.
- Antenna shall be installed also according to antenna manufacture instructions.

WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect CL865 or customer specific requirements from ESD event to Antenna port (pin 34).

8. Logic level specifications

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels. The following table shows the logic level specifications used in the CL865 interface circuits:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) when on	-0.3V	+2.3V

Operating Range - Interface levels (1.8V CMOS)

Level	Min	Max
Input high level	1.5V	2.1V
Input low level	0V	0.35V
Output high level	1.35V	1.8V
Output low level	0V	0.45V

Current characteristics

Level	Typical
Output Current	2mA
Input Current	30uA

8.1. Reset signal

Signal	Function	I/O	Pad
RESET*	Phone reset	I	47

RESET* is used to reset the CL865. Whenever this signal is pulled low, the CL865 is reset. When the device is reset it stops any operation. After the release of the reset CL865 is unconditionally shut down, without doing any detach operation from the network where it is registered. This behavior is not a proper shut down because any CDMA device is requested to issue a detach request on turn off. For this reason the Reset signal must not be used to normally shutting down the device, but only as an emergency exit in the rare case the device remains stuck waiting for some network response.

The RESET* is internally controlled on start-up to achieve a proper power-on reset sequence, so there's no need to control this pin on start-up. It may only be used to reset a device already on that is not responding to any command.

NOTE:

Do not use this signal to power OFF the CL865. Use the ON/OFF procedure to perform this function.

Reset Signal Operating levels:

Signal	Min	Max
RESET* Input high	1.5V(NOTE1)	1.9V
RESET* Input low	0V	0.35V

(NOTE1) this signal is internally pulled up so the pin can be left floating if not used.

If unused, this signal may be left unconnected. If used, then it must always be connected with an open collector transistor, to permit to the internal circuitry the power on reset and under voltage lockout functions.

9. USB Port

The CL865 module includes a Universal Serial Bus (USB) transceiver, which operates at USB Full-speed (12Mbits/sec) and slave mode only.

It is compliant with the USB 2.0 specification and can be used for diagnostic monitoring, control and data transfers.

The table below describes the USB interface signals:

Pad	Signal	I/O	Function	Type
18	USB_D+	I/O	USB differential Data(+)	
17	USB_D-	I/O	USB differential Data(+)	
16	USB_VUSB	I	Power for the internal USB transceiver	5V

The USB_DPLUS and USB_DMINUS signals have a clock rate of 60MHz. The signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized. The impedance value should be as close as possible to 100 Ohms differential.

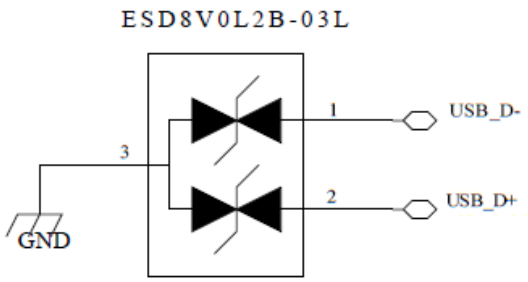
The table below describes the VUSB specification:

Parameter	Min	Max
Input voltage	4.4V	5.0V
Input current	50mA	-

WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect CL865 or customer specific requirements from ESD event to USB lines (Pin16, Pin17 and Pin18).

In case there is a need to add an ESD protection the suggested connection is the following:



10. Serial Port

The serial ports on the Telit CL865 are the interface between the module and OEM hardware.

2 serial ports are available on the module:

- Modem Serial Port 1 (Main)
- Modem Serial Port 2 (Auxiliary)

Several configurations can be designed for the serial port on the OEM hardware.

The most common are:

- RS232 PC comport
- Microcontroller UART@1.8V(Universal Asynchronous Receiver Transmit)
- Microcontroller UART@5V or other voltages different from 1.8V

Depending on the type of serial port on the OEM hardware, a level translator circuit may be needed to make the system work.

On the CL865 the ports are CMOS 1.8V.

The electrical characteristics of the serial port are explained in the following tables:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on non-power pin with respect to ground	-0.3	+2.3V

Operating Range - Interface levels (1.8V CMOS)

Parameter	Min	Max
Input high level	1.5V	2.1 V
Input low level	0V	0.35V
Output high level	1.35V	1.8V
Output low level	0V	0.45V

10.1.Modem Serial Port 1

The serial port 1 on the CL865 is a +1.8V UART with all 7 RS232 signals.

It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

RS232 Pin #	Signal	CL865 Pad No.	Function	Usage
1	C109/DCD	1	Data Carrier Detect	Output from the CL865 that indicates the carrier presence
2	C104/RXD	8	Transmit line *see Note	Output transmit line of the CL865 UART
3	C103/TXD	7	Receive line *see Note	Input receive of the CL865 UART
4	C108/DTR	4	Data Terminal Ready	Input to the CL865 that controls the DTE READY condition
5	GND	-	-	GND
6	C107/DSR	3	Data Set Ready	Output from the CL865 that indicates the module is ready
7	C106/CTS	6	Request to Send	Output from the CL865 that controls the hardware flow control
8	C105/RTS	5	Clear to Send	Input to the CL865 that controls the hardware flow control
9	C125/RING	2	Ring Indicator	Output from the CL865 that indicates the incoming call condition

The following table shows the typical value (pulled inside the baseband chipset) and status for input lines in all module states:

Signal/State	OFF	RESET	ON	Power saving	PU tied to
TXD	unknown	Pull Down (21K~210K)	Pull Up (39K~390K)	Pull Up (39K~390K)	1.8V
RTS		Pull Down (21K~210K)			
DTR		Pull Up (39K~390K)			

NOTE:

According to V.24, RX/TX signal names are referred to the application side. Therefore, on the CL865 side these signals are on the opposite direction:

TXD on the application side will be connected to the receive line (here named C103/TXD)

RXD in the application side will be connected to the transmit line (here named C104/RXD)

NOTE:

For minimum implementation, only the TXD and RXD lines must be connected, the other lines can be left open provided a software flow control is implemented.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CL865 when the module is powered off or during an ON/OFF transition.

NOTE:

High-speed UART supports up to 4Mbps. Please refer to the AT command User Guide in detail.

WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect CL865 or customer specific requirements from ESD event to UART port (Pin5, Pin6, Pin7 and Pin8).

10.2.Modem Serial Port 2

The secondary serial port on the CL865 is a CMOS 1.8V with only RX and TX signals.

The signals of the CL865 serial port are:

CL865 Pad No.	Signal	I/O	Function	Type
45	TXD_AUX	O	Auxiliary UART (TX data to DTE)	CMOS 1.8V
44	RXD_AUX	I	Auxiliary UART (RX data from DTE)	CMOS 1.8V

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the CL865 when the module is powered off or during an ON/OFF transition.

10.3.RS232 Level Translation

In order to interface the Telit CL865 with a PC com port or a RS232 (EIA/TIA-232) application, a level translator is required. This level translator must:

- Invert the electrical signal in both directions
- Change the level from 0/1.8V to +/-15V

Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required. The simplest way to translate the levels and invert the signal is by using a single chip level translator. There is a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards). By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.

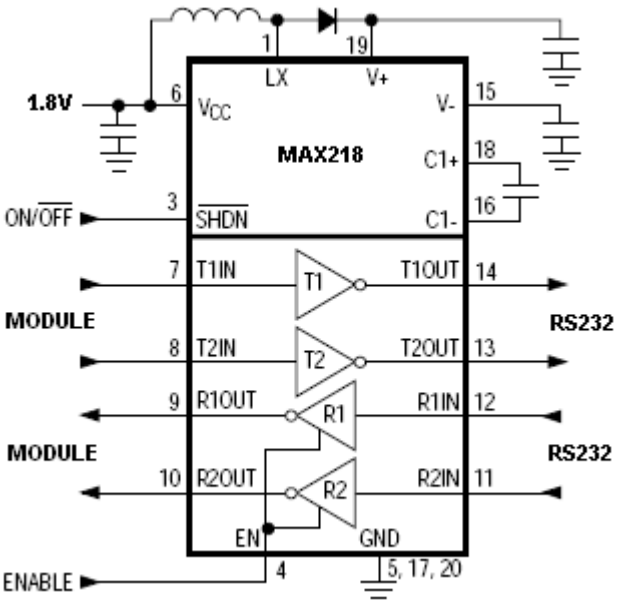
In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers

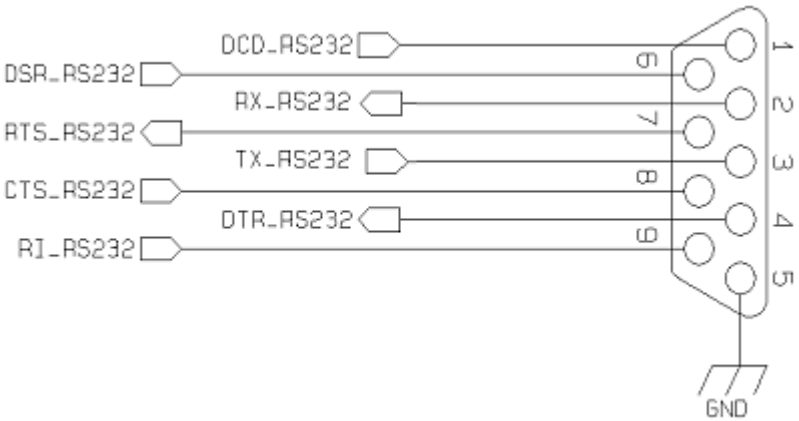
NOTE:

The digital input lines working at 1.8V CMOS have an absolute maximum input voltage of 2.1V; therefore the level translator IC shall not be powered by the +3.8V supply of the module. Instead, it must be powered from a +1.8V (dedicated) power supply.

An example of RS232 level adaption circuitry could be accomplished using a MAXIM transceiver (MAX218).
In this case the chipset is capable of translating directly from 1.8V to the RS232 levels (Example on 4 signals only).



The RS232 serial port lines are usually connected to a DB9 connector with the following layout:

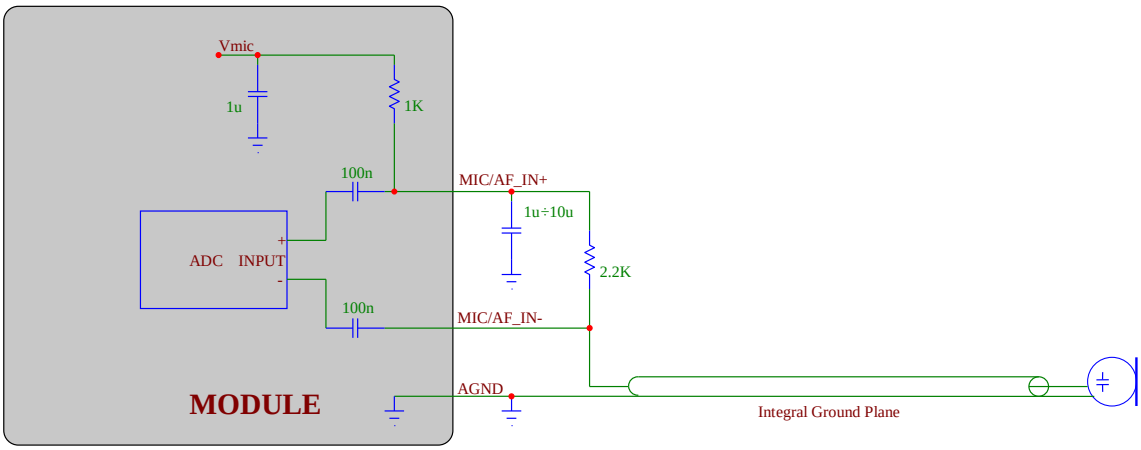


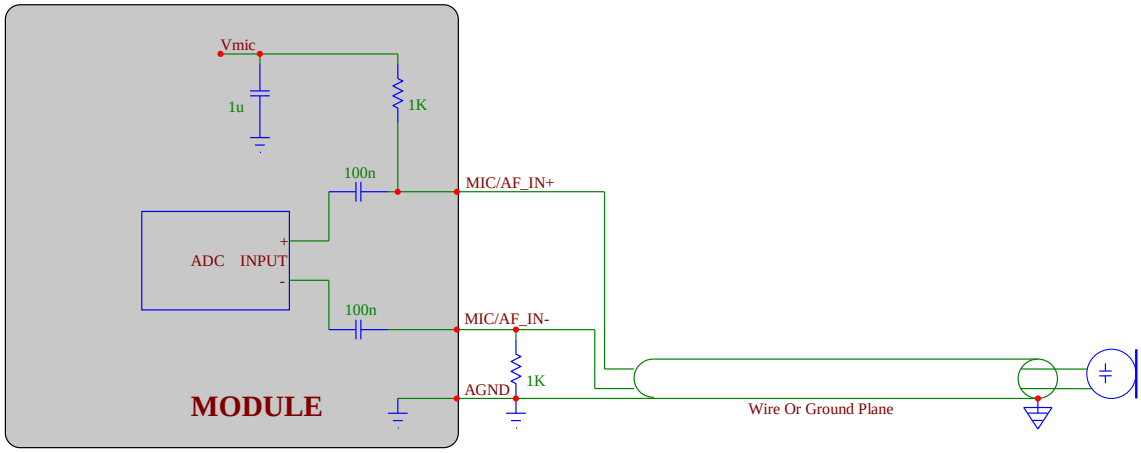
11. Audio Section Overview

The Base Band Chip of the CL865 provides one input for audio to be transmitted (*Uplink*), that can be connected directly to a microphone or an audio source.
The bias for the microphone is already provided by the product; so the connection can be done in both following ways:

For more information refer to Telit document: "80000NT10007a Audio Settings Application Note ".

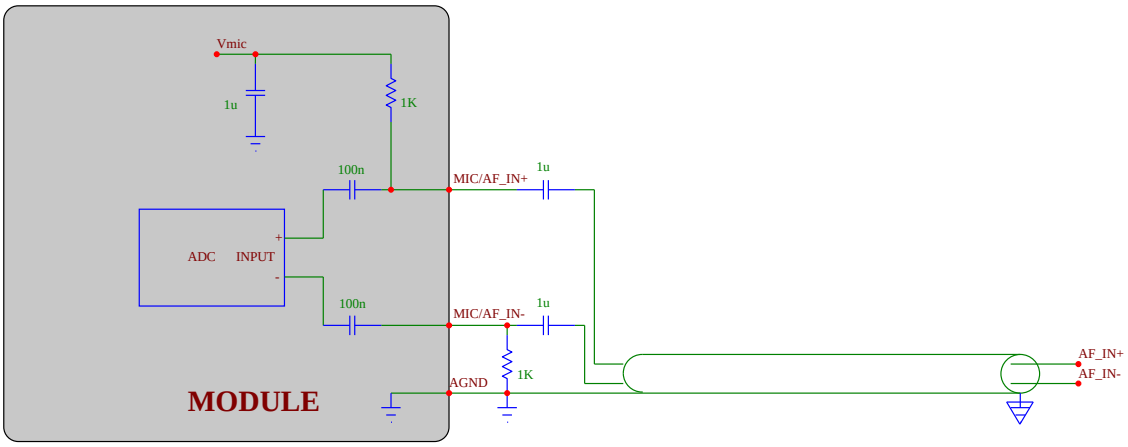
MIC connection

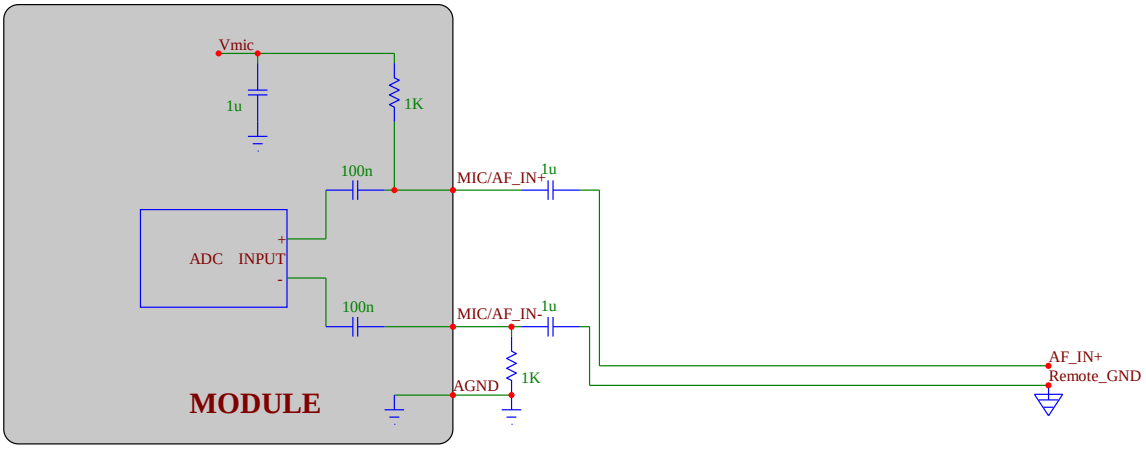




TIP: Since the J-FET transistor inside the microphone acts as RF-detector-amplifier, ask vendor for a microphone with anti-EMI capacitor (usually a 33pF or a 10pF capacitor placed across the output terminals inside the case).

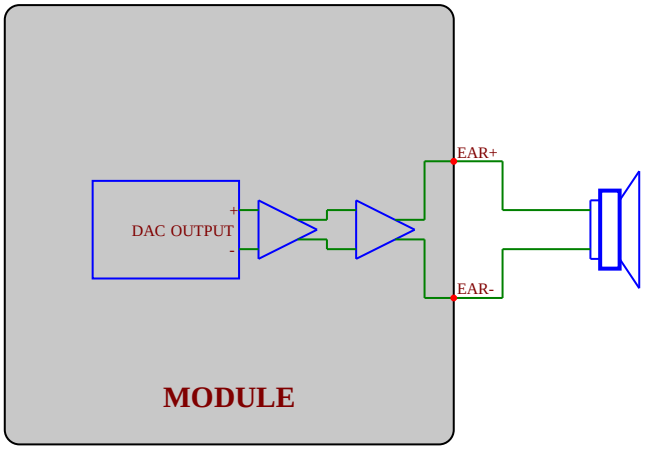
LINE-IN connection





If the audio source is not a mike but a different device, the following connections can be done. Place a 1Kohm resistor to ground on the negative input, in order to get balanced the input; than connect the source via 1uF capacitor, so the DC current is blocked.
Since the input is differential, the common mode voltage noise between the two (different) grounds is rejected, provided that both AF_IN+ & AF_IN- are connected directly onto the source.

EAR connection



The audio output of the CL865 is balanced, this is helpful to double the level and to reject common mode (click and pop are common mode and therefore rejected).
These outputs can drive directly a small loudspeaker with electrical impedance not lower than 32Ohm.

TIP: in order to get the maximum audio level at a given output voltage level (dBspl/Vrms), the following breaking through procedure can be used. Have the loudspeaker as close as you can to the listener (this simplify also the echo cancelling); choose the loudspeaker with the higher sensitivity (dBspl per W); choose loudspeakers with the impedance close to the limit, in order to feed more power inside the transducer (it increases the W/Vrms ratio). If this were not enough, an external amplifier should be used.

11.1. Digital Voice Interface (DVI)

The product is providing one Digital Audio Interface (DVI) on the following Pins:

Pad	Signal	I/O	Function	Type
42	DVI_WA0	I/O	Digital Voice interface (WA0)	1.8V
41	DVI_RX	I	Digital Voice interface (RX)	
40	DVI_TX	O	Digital Voice interface (TX)	
39	DVI_CLK	I/O	Digital Voice interface (CLK)	

11.1.1. CODEC Example

Please refer to the Digital Voice Interface Application note.

12. General Purpose I/O

The CL865 module is provided by a set of Digital Input / Output pins

Input pads can only be read; they report the digital value (high or low) present on the pad at the read time.

Output pads can only be written or queried and set the value of the pad output.

An alternate function pad is internally controlled by the CL865 firmware and acts depending on the function implemented.

The following GPIOs are available on the CL865:

Pad	Signal	I/O	Function	Type	Default State	Note
42	GPIO_01	I/O	Configurable GPIO	CMOS 1.8V	INPUT	Alternate function DVI_WA0
41	GPIO_02	I/O	Configurable GPIO	CMOS 1.8V	INPUT	Alternate function DVI_RX
40	GPIO_03	I/O	Configurable GPIO	CMOS 1.8V	INPUT	Alternate function DVI_TX
39	GPIO_04	I/O	Configurable GPIO	CMOS 1.8V	INPUT	Alternate function DVI_TX
29	GPIO_05	I/O	Configurable GPIO	CMOS 1.8V	INPUT	
28	GPIO_06	I/O	Configurable GPIO	CMOS 1.8V	INPUT	Alternate function ALARM
27	GPIO_07	I/O	Configurable GPIO	CMOS 1.8V	INPUT	Alternate function
26	GPIO_08	I/O	Configurable GPIO	CMOS 1.8V	INPUT	Alternate function STAT_LED

WARNING:

During power up the GPIOs may be subject to transient glitches.

12.1.GPIO Logic Levels

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels.

The following table shows the logic level specifications used in the CL865 interface circuits:

Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) when on	-0.3V	+2.3V

Operating Range - Interface levels (1.8V CMOS)

Level	Min	Max
Input high level	1.5V	2.1V
Input low level	0V	0.35V
Output high level	1.35V	1.8V
Output low level	0V	0.45V

Current characteristics

Level	Typical
Output Current	2mA
Input Current	30uA

12.2.Using a GPIO Pad as Input

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

If the digital output of the device to be connected with the GPIO input pad has interface levels different from the 1.8V CMOS, then it can be buffered with an open collector transistor with a 47KΩ pull-up resistor to 1.8V.

NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

12.3.Using a GPIO Pad as Output

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.

12.4.Using the Alarm Output GPIO6

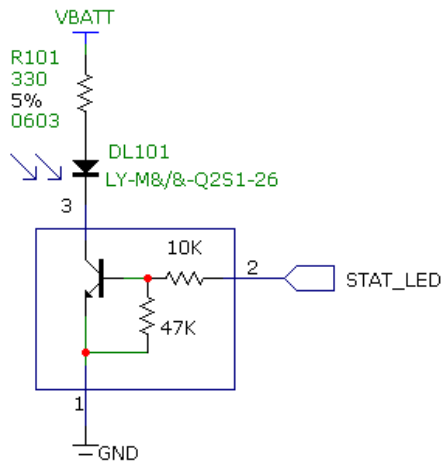
The GPIO6 pad, when configured as Alarm Output, is controlled by the CL865 module and will rise when the alarm starts and fall after the issue of a dedicated AT command.
This output can be used to controlling microcontroller or application at the alarm time.

12.5.Indication of Network Service Availability

The STAT_LED pin status shows information on the network service availability and Call status. In the CL865 modules, the STAT_LED usually needs an external transistor to drive an external LED. Because of the above, the status indicated in the following table is reversed with respect to the pin status:

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active

A schematic example could be:



12.6.RTC Bypass Output

The VRTC pin brings out the Real Time Clock supply but it is NOT separate from the rest of the digital part. So unlike other Telit's products, CL865 cannot support RTC function if VBATT is not supplied.

In summary in order to use RTC function with CL865 VBATT must be supplied from the application.

VRTC also supplies reference power to help CL865 check the time from SMPL (Sudden Momentary Power Loss).

So it is recommended as best practice to connect VRTC to a shunt capacitor (VRTC to GND) and the acceptable capacitor value is:

Parameter	Min
Keep-alive capacitor on Pad no. = 30	6.8uF

NOTE:

VBATT must be supplied in order to use RTC function.

NOTE:

It is recommended to add a keep-alive capacitor on VRTC.

WARNING:

NO devices must be powered from this pin.

12.7.VAUX/PWRMON Power Output

A regulated power supply output is provided in order to supply small devices from the module. This output is active when the module is ON and goes OFF when the module is shut down. The operating range characteristics of the supply are:

Operating Range – VAUX/PWRMON power supply

Parameter	Min	Typical	Max
Output voltage	1.77V	1.8V	1.83V
Output current			100mA
Output bypass capacitor (Inside the module)		2.2µF	

13. DAC and ADC Section

13.1.DAC converter

13.1.1. Description

The CL865 module provides a Digital to Analog Converter. The signal (named DAC_OUT) is available on pin 15 of the CL865 module.

The on board DAC is in the range from 0 to 1023. However, an external low-pass filter is necessary.

Parameter	Min	Max	Units
Voltage range (filtered)	0	1.8	Volt
Range	0	1023	Steps

The precision is 1023 steps, so since the maximum voltage is 1.8V, the integrated voltage could be calculated with the following formula:

Integrated output voltage = 1.8 * value / 1023

DAC_OUT line must be integrated (for example with a low band pass filter) in order to obtain an analog voltage.

13.1.2. Enabling DAC

An AT command is available to use the DAC function.

The command is: AT#DAC[=<enable>[,<value>]]

<value> - scale factor of the integrated output voltage (0..1023 ~ 10 bit precision)

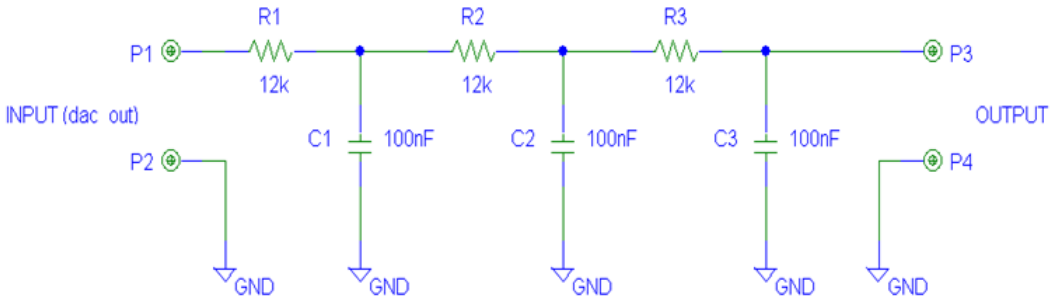
it must be present if <enable>=1

Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

NOTE:

The DAC frequency is selected internally. D/A converter must not be used during POWERSAVING.

13.1.3. Low Pass Filter Example



13.2.ADC converter

13.2.1. Description

The on board ADC is 12-bit converter. It is able to read a voltage level in the range of 0 ~ 1.2 volts applied on the ADC pin input and store and convert it into 12 bit word.

Parameter	Min	Max	Units
Input Voltage range	0	1.2	Volt
AD conversion	-	12	bits
Resolution	-	< 1	mV
Input Resistance	1		Mohm

The signal is available on the following pads:

PAD	Name	I/O	Description	Notes
13	ADC_IN1	AI	Analog/Digital converter input	Accepted values 0 to 1.2V DC
14	ADC_IN2	AI	Analog/Digital converter input	Accepted values 0 to 1.2V DC

NOTE:

If the ADC_IN1 or ADC_IN2 is open (has no input voltage), the ADC value from the open port should not be used.

13.2.2. Using ADC Converter

An AT command is available to use the ADC function.

The command is ***AT#ADC=1,2***

The read value is expressed in mV

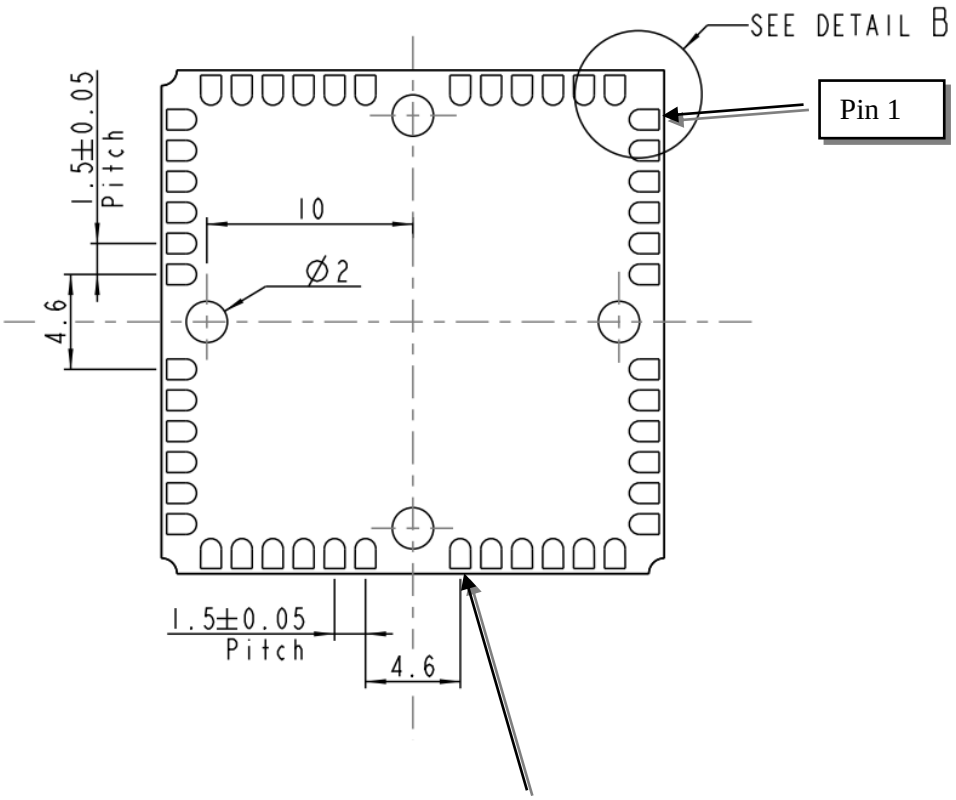
Refer to SW User Guide or AT Commands Reference Guide for the full description of this function.

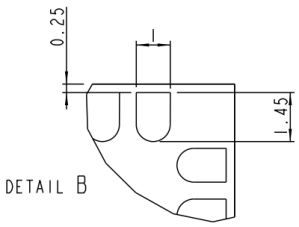
14. Mounting the CL865 on your Board

14.1. General

The CL865 modules have been designed to be compliant with a standard lead-free SMT process.

14.2. Module finishing & dimensions



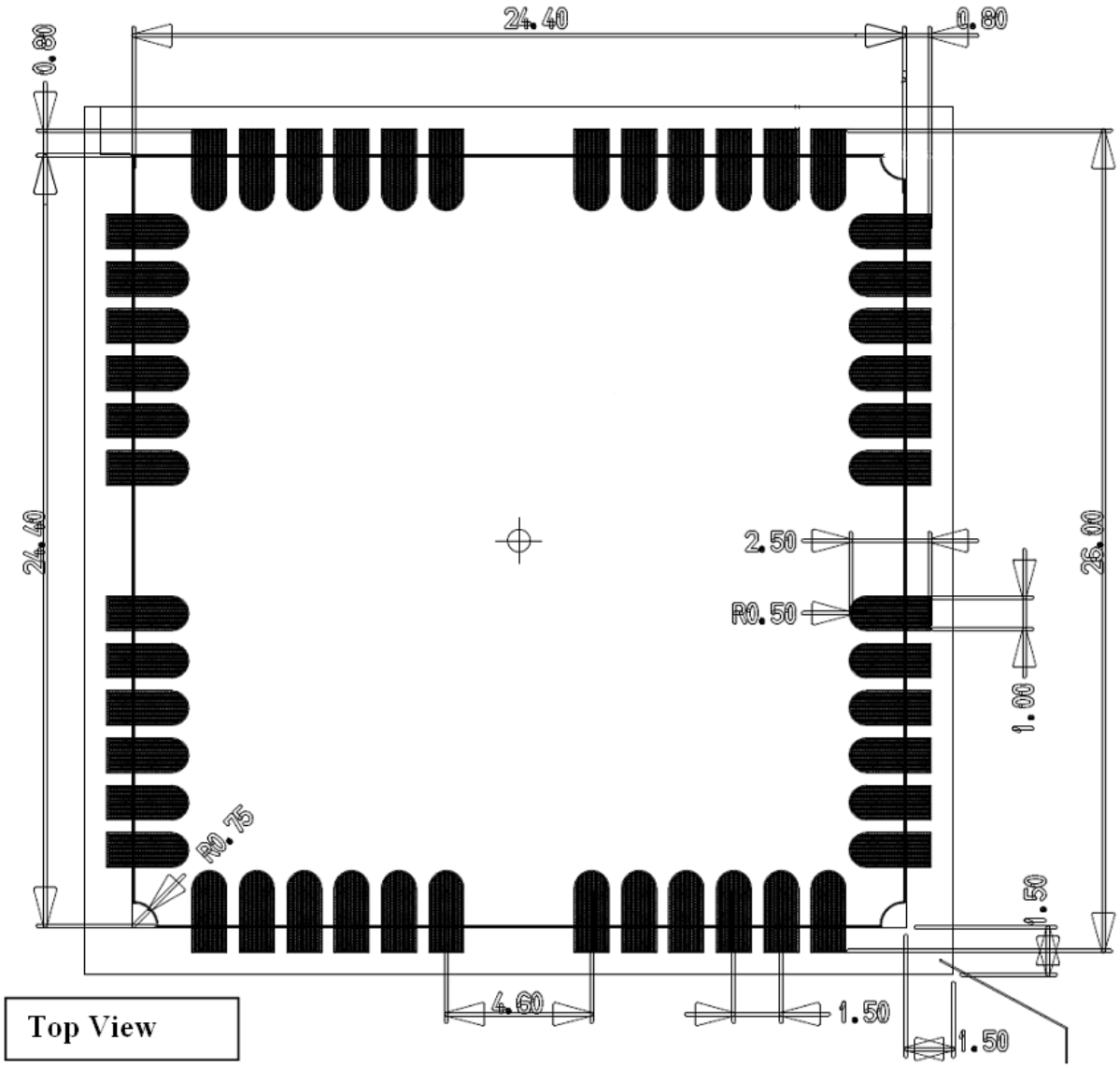


Lead-free Alloy:
Surface finishing Ni/Au for all solder pads

Bottom View

Dimensions in mm

14.3.Recommended foot print for the application



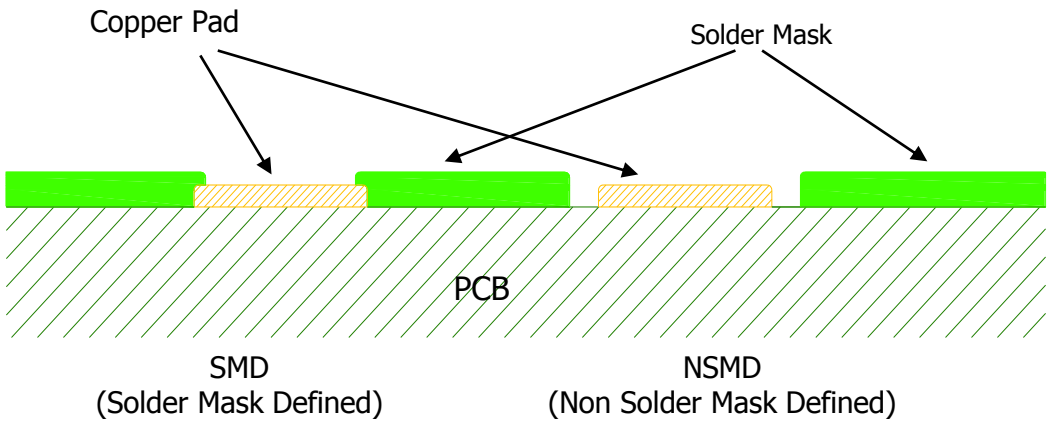
In order to easily rework the CL865 is suggested to consider on the application a 1.5 mm placement inhibited area around the module.
It is also suggested, as common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.

14.4.Stencil

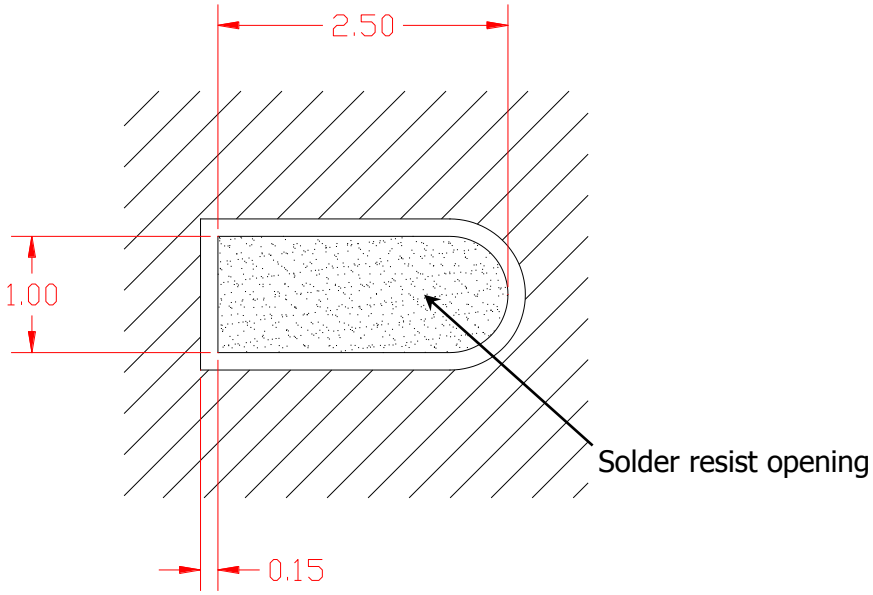
Stencil's apertures layout can be the same of the recommended footprint (1:1), we suggest a thickness of stencil foil ≥ 120µm.

14.5.PCB pad design

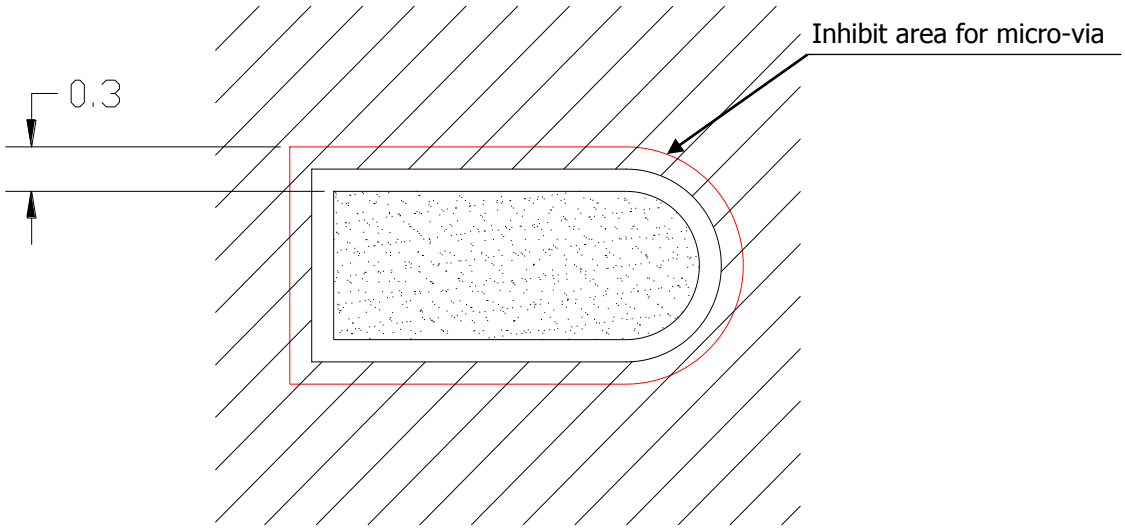
Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.



14.6.Recommendations for PCB pad dimensions(mm):



It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal of the pad itself (see following figure).



Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB pad surfaces:

Finish	Layer thickness [µm]	Properties
Electro-less Ni / Immersion Au	3 –7 / 0.05 – 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.

It is not necessary to panel the application PCB, however in that case it is suggested to use milled contours and predrilled board breakouts; scoring or v-cut solutions are not recommended.

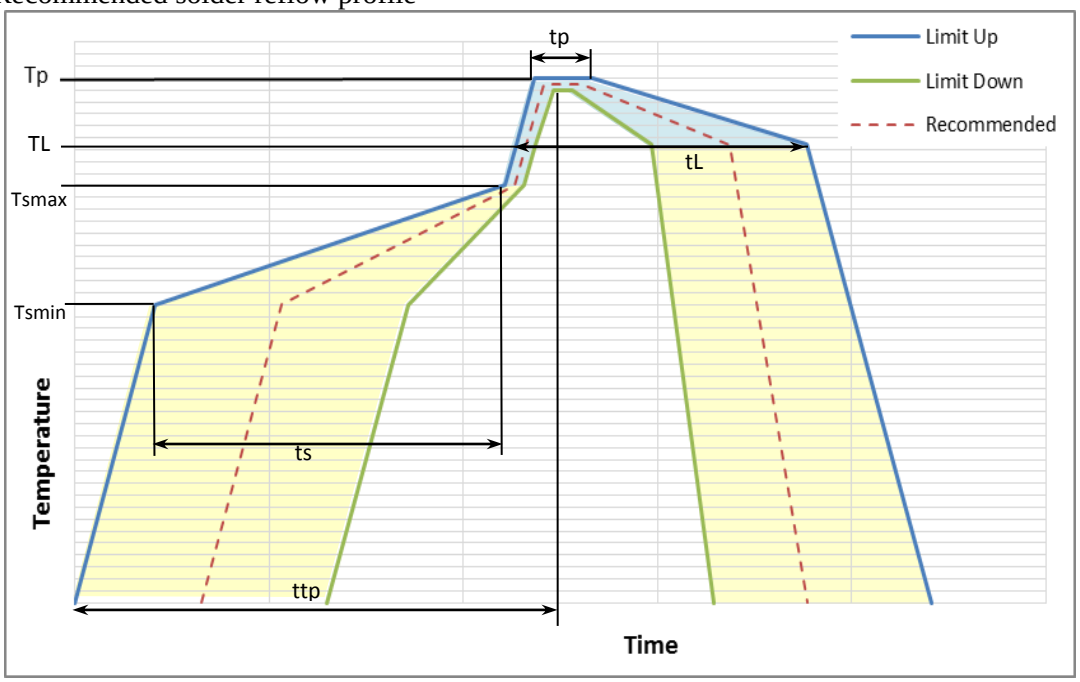
14.7.Solder paste

	Lead free
Solder paste	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

14.8.CL865 Solder reflow

Recommended solder reflow profile



Profile Feature	Pb-Free Assembly
Average ramp-up rate (TL to TP)	3°C/second max
Preheat – Temperature Min (Tsmin) – Temperature Max (Tsmax) – Time (min to max) (ts)	 150°C 200°C 60-180 seconds
Tsmax to TL – Ramp-up Rate	 3°C/second max
Time maintained above: – Temperature (TL) – Time (tL)	 217°C 60-150 seconds
Peak Temperature (Tp)	245 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds
Ramp-down Rate	6°C/second max.
Time 25°C to Peak Temperature (ttp)	8 minutes max.

NOTE:

All temperatures refer to topside of the package, measured on the package body surface

WARNING:

The CL865 module withstands one reflow process only.

14.9.Debug of the CL865 in production

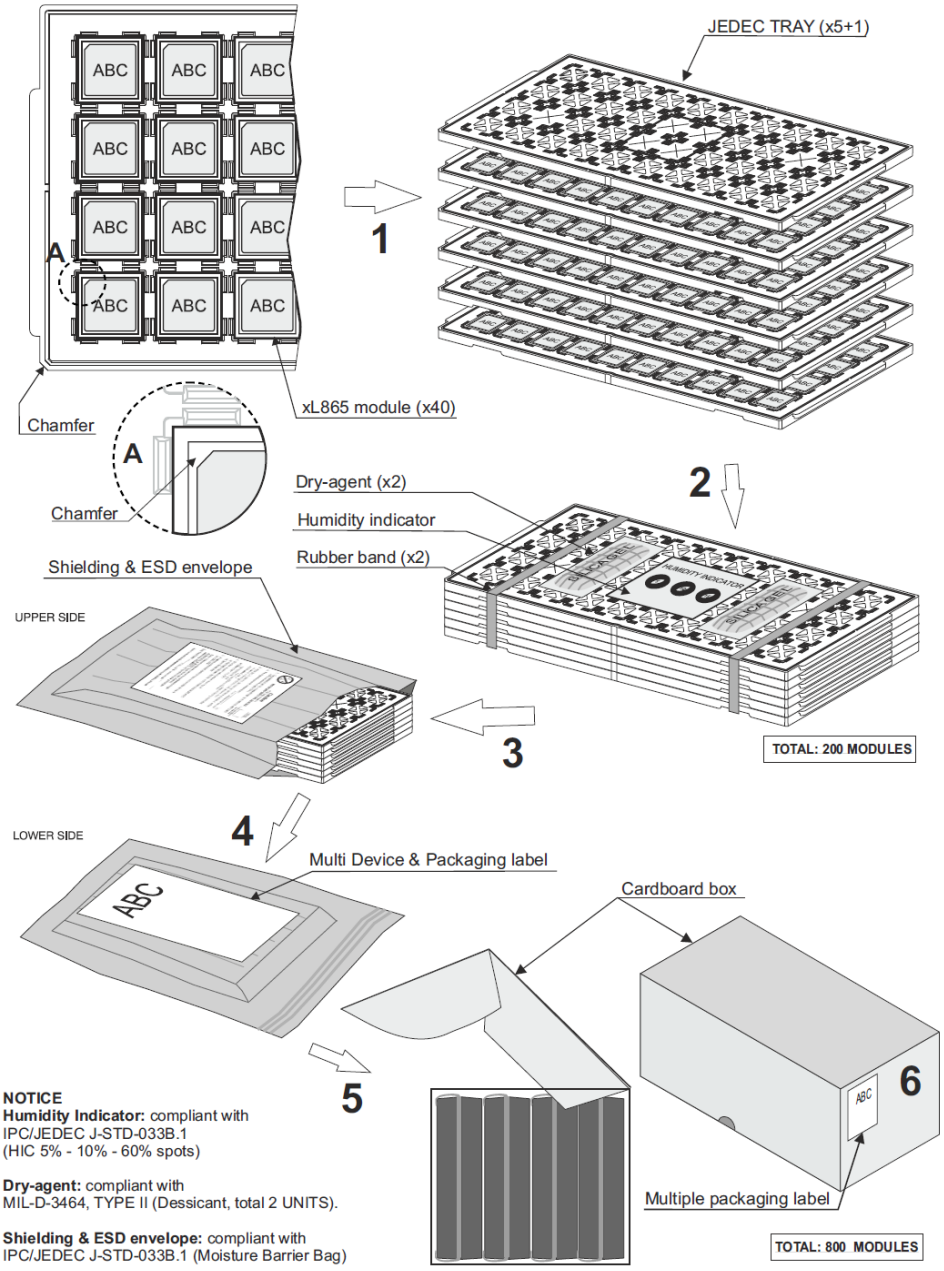
To test and debug the mounting of the CL865, we strongly recommend foreseeing test pads on the host PCB, in order to check the connection between the CL865 itself and the application and to test the performance of the module connecting it with an external computer. Depending by the customer application, these pads include, but are not limited to the following signals:

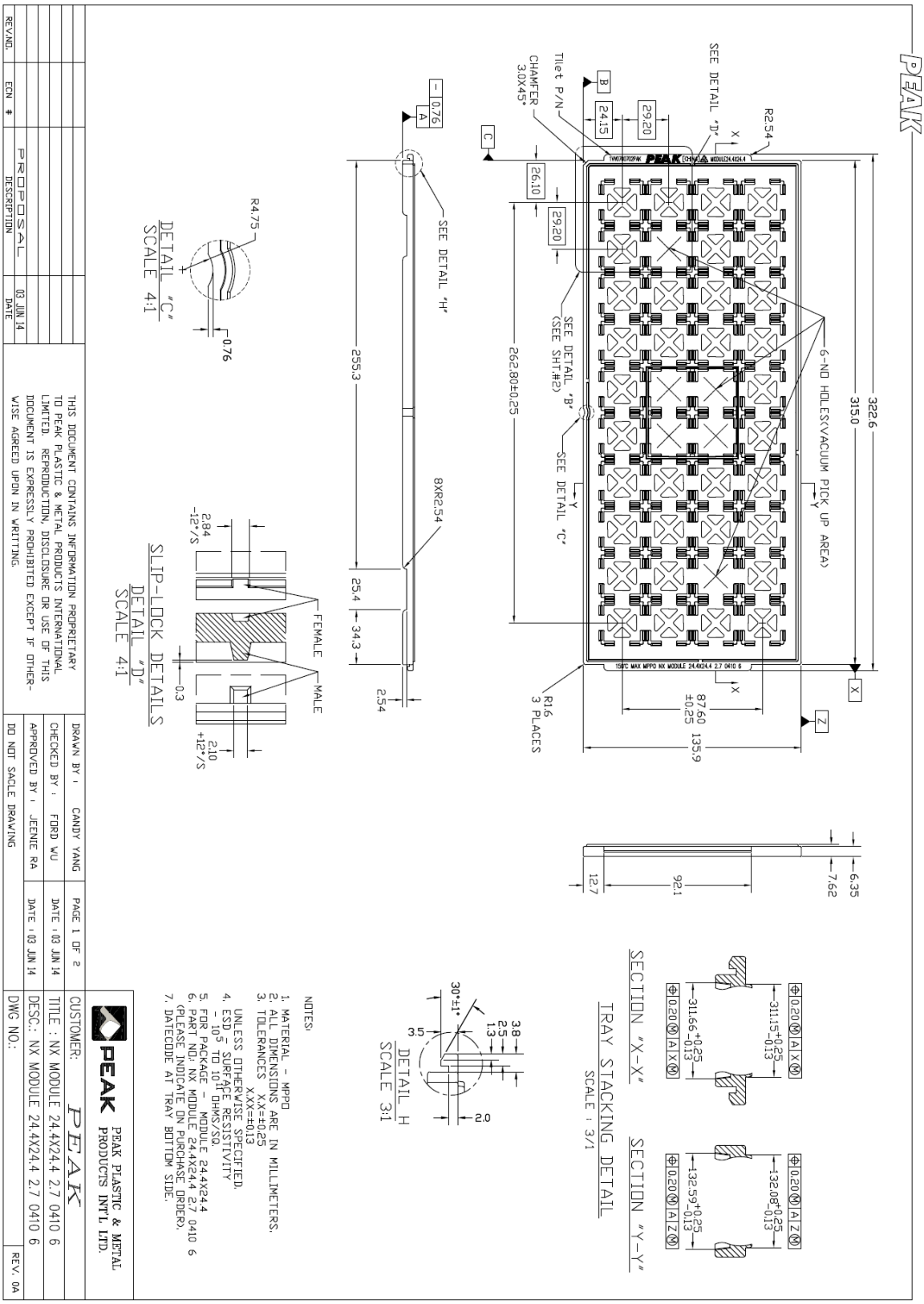
TXD
RXD
RESET*
GND
VBATT
VBATT_PA
TXD_AUX
RXD_AUX
PWRMON

15. Packing system

15.1. Packing on tray

The CL865 modules are packaged on trays of ***40*** pieces each. These trays can be used in SMT processes for pick & place handling.




PEAK
SEE DETAIL "D"
Tilet P/N
CHAMFER 3.0X45°
SEE DETAIL "B" (SEE SHT#2)
SEE DETAIL "C"
SEE DETAIL "H"
6-NO HOLES(VACUUM PICK UP AREA)
322.6
315.0
262.80±0.25
255.3
87.60 ±0.25
135.9
R16 3 PLACES
R2.54
8XR2.54
DETAIL "C" SCALE 4:1
R4.75
0.76
SLIP-LOCK DETAILS
DETAIL "D" SCALE 4:1
FEMALE
MALE
2.84 -12°/S
2.10 +12°/S
0.3
DETAIL H SCALE 3:1
30°±1°
3.8
2.5
1.3
3.5
2.0
SECTION "X-X"
SECTION "Y-Y"
TRAY STACKING DETAIL
SCALE : 3/1
12.7
92.1
7.62
6.35
NOTES:
1. MATERIAL - MPPO
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. TOLERANCES X.XX=±0.25
X.XXX=±0.13
UNLESS OTHERWISE SPECIFIED.
4. ESD: SURFACE RESISTIVITY
10^5 TO 10^11 OHMS/SQ.
5. FOR PACKAGE - MODULE 24.4X24.4
6. PART NO: NX MODULE 24.4X24.4 2.7 0410 6
(PLEASE INDICATE ON PURCHASE ORDER).
7. DATECODE AT TRAY BOTTOM SIDE.
THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO PEAK PLASTIC & METAL PRODUCTS INTERNATIONAL LIMITED. REPRODUCTION, DISCLOSURE OR USE OF THIS DOCUMENT IS EXPRESSLY PROHIBITED EXCEPT IF OTHERWISE AGREED UPON IN WRITTING.
DRAWN BY : CANDY YANG
CHECKED BY : FORD WU
APPROVED BY : JEENIE RA
DATE : 03 JUN 14
PAGE 1 OF 2
DO NOT SACLE DRAWING
PEAK PLASTIC & METAL PRODUCTS INT'L LTD.
CUSTOMER: PEAK
TITLE : NX MODULE 24.4X24.4 2.7 0410 6
DESC.: NX MODULE 24.4X24.4 2.7 0410 6
DWG NO.:
REV. 0A
REV.NO. | ECN # | DESCRIPTION | DATE
PROPOSAL | 03 JUN 14

15.2. Moisture sensibility

The level of moisture sensibility of the Product is "3" according with standard IPC/JEDEC J-STD-020, take care of all the relative requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) The shelf life of the Product inside of the dry bag must be 12 months from the bag seal date, when stored in a non-condensing atmospheric environment of <40°C / 90% RH
b) Environmental condition during the production: <= 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5
c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected
d) Baking is required if conditions b) or c) are not respected
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more

16. Application Design Guide

16.5. Download and Debug Port

One of the following options should be chosen in the design of host system in order to download or upgrade the Telit's software and debug CL865 when CL865 is already mounted on a host system.

CASE I:
Users who use both of UART and USB interfaces to communicate with CL865
- Must implement a download method in a host system for upgrading CL865 when it's mounted.

CASE II:
Users who use USB interface only to communicate with CL865
- Must arrange UART port in a host system for debugging or upgrading CL865 when it's mounted.

CASE III:
Users who use UART interface only to communicate with CL865
- Must arrange USB port in a host system for debugging or upgrading CL865 when it's mounted.

17. Certifications and Conformity (Certifications et Conformité)

The CL865 is FCC/IC Approved as module to be installed in other devices. This device should be used only for fixed and mobile applications and if the final product after integration is intended for portable use, a new application and FCC is required.

Le CL865 est approuvé FCC/IC comme module à installer dans d'autres dispositifs. Ce dispositif doit être utilisé uniquement pour des applications fixes et mobiles et si le produit fini est prévu après intégration pour un usage portatif, une nouvelle application et la FCC est requise

The user is cautioned that this device should be used only as specified within this manual to meet RF exposure requirements.

L'utilisateur est averti que ce dispositif doit être utilisé uniquement comme spécifié dans ce manuel pour répondre aux normes d'exposition aux ondes rf.

Use of this device in a manner inconsistent with this manual could lead to excessive RF exposure conditions.

L'utilisation de ce dispositif en quelque sorte contradictoire avec ce manuel a pu mener aux états excessifs d'exposition de rf.

The CL865 is conforming to the following US Directives:

- Use of RF Spectrum. Standards: FCC47 Part 22, 24 & 90
- EMC Standards: FCC47 Part 15

Le CL865 est conforme aux directives suivantes des USA

- Utilisation de spectre de rf. Normes : FCC47 partie 22, 24 &90
- Normes d'EMC : FCC47 partie 15

This device complies with Part 15 of the FCC Rules.

Ce dispositif est conforme à la partie 15 des règles FCC.

Operation is subject to the following two conditions:

(1) This device may not cause harmful interference, and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le fonctionnement est sujet aux deux conditions suivantes :

(1) ce dispositif peut ne pas causer l'interférence nocive, et

(2) ce dispositif doit accepter aucune interférence, y compris un interférence qui pourrait causer le fonctionnement non désiré du dispositif.

The user must refer to below information to meet the FCC/IC's RF exposure rules and regulations when they design:

Lors de la conception, l'utilisateur doit se référer à l'information ci-dessous pour remplir les conditions et règlementations FCC/IC' d'exposition aux ondes RF:

- The system antenna(s) used for this transmitter must be installed to provide a separation distance of at least 20 cm from all the persons and must not be co-located or operating in conjunction with any other antenna or transmitter.
  Le système d'antenne utilisé pour cet émetteur doit être installé à une distance d'au moins de 20 cm de toute personne et ne doit pas être co-implanté ou opérer en même temps que n'importe quelle autre antenne ou émetteur.

- The system antenna(s) used for this module must not exceed 5.12dBi in CDMA BC0&BC10 and 6.12dBi in CDMA BC1 for mobile and fixed or mobile operating configurations.
  Le système d' antenne utilisé pour ce module ne doit pas dépasser 5.12dBi en CDMA BC0&BC10 et 6.12dBi en CDMA BC1 pour des configurations mobiles et fixes ou des configurations opérant en mode mobile.

- Users and installers must be provided with antenna installation instructions and transmitter operating conditions for satisfying RF exposure compliance.
  Manufacturers of mobile, fixed or portable devices incorporating this module are advised to clarify any regulatory questions and to have their complete product tested and approved for FCC compliance.
  Les instructions d'installation de l'antenne ainsi que les conditions de fonctionnement de l'émetteur doivent être remis aux utilisateurs et aux installateurs conformément à la règlementation sur l'exposition aux ondes rf. Des fabricants des dispositifs mobiles, fixes ou portables incorporant ce module sont invités à clarifier toutes les questions de normalisation et à avoir leur produit complètement testé pour la mise en conformité FCC.

- CL865 is intended for the OEM integrator only.
  CL865 est prévu pour l'intégrateur OEM seulement.

- The user is required to see the Grant of Equipment document for other restrictions.
  L'utilisateur doit se referrer au document « Grant of Equipment » pour d'autres restrictions.

- CL865 must be operated and used with a locally approved access point.
  CL865 doit être actionné et utilisé avec un point d'accès localement approuvé.

- The radio transmitter(IC ID: 5131A- CL865DUAL) has been approved by Industry Canada to operate with the antenna type listed in this manual with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

L'émetteur radio (identification d'IC : 5131A- CL865DUAL) a été approuvé par Industry Canada pour fonctionner avec le type d'antenne énuméré dans ce manuel avec le gain autorisé maximum et l'impédance d'antenne exigée pour chaque type d'antenne indiqué. Les types d'antenne non inclus dans cette liste, ayant un gain supérieur au gain maximum indiqué pour ce type, sont strictement interdits pour un usage avec ce dispositif.

The following regulatory and safety notices must be published in documentation supplied to the end user of the product or system incorporating an adapter in compliance with local regulations.

- Host system including CL865 must be labeled with
  "Contains transmitter module with
  FCC ID: RI7CL865-DUAL and IC ID: 5131A-CL865DUAL"

Les notices de normalisation et de sécurité doivent se trouver dans la documentation fournie à l'utilisateur du produit ou du système incorporant un adaptateur conforme aux règlementations locales.

- Le système hôte comprenant CL865 doit être marqué avec « Contient un module émetteur avec IDENTIFICATION FCC : RI7CL865-DUAL et identification IC : 5131A-CL865DUAL »

18. Safety Recommendations

READ CAREFULLY

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:

- Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc.
- Where there is risk of explosion such as gasoline stations, oil refineries, etc. It is the responsibility of the user to enforce the country's regulations and the specific environmental regulation.

Do not disassemble the product; any evidence of tampering will compromise the warranty validity. Follow the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to conform to the security and fire prevention regulations. The product has to be handled with care, avoiding any contact with the pads because electrostatic discharges may damage the product itself.

The system integrator is responsible for the functioning of the final product; therefore, care has to be taken with the external components of the module as well as of any project or installation issue because of the risk of disturbing the CDMA network or external devices or having impact on security. Should there be any doubt, please refer to the technical documentation and the regulations in force. Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case this requirement cannot be satisfied, the system integrator has to assess the final product against SAR regulations.

19. Document History

Revision	Date	Changes
0	2013-12-10	Initial release
1	2014-07-01	Updated 2.2 Product Specifications Updated 4.1 PIN-OUT Updated 5.1 Auto-Turning ON the CL865 Updated 5.2 Turning OFF the CL865 Updated 5.3 Hardware Unconditional Shutdown Updated 6.2 Power Consumption Updated 7.1 CDMA Antenna Requirements Added 10.1.2 LINE-IN Connection Updated 12.2 ADC Converter Added 16 Conformity Assessment Issues
2	2015-05-22	Added information for CL865-SC Updated Chapters 5, 6, 7.1, 8, 11, 12.6, 15.1