

# DE910 Series Hardware User Guide

1w0300951 Rev.9 – 2016-09-14









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# 1. Introduction

## 1.1. Scope

The aim of this document is the description of typical hardware solutions useful for developing a product with the Telit DE910 module.

## 1.2. Audience

This document is intended for Telit customers who are about to implement their applications using our DE910 modules.

## 1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

[TS-EMEA@telit.com](mailto:TS-EMEA@telit.com)  
[TS-NORTHAMERICA@telit.com](mailto:TS-NORTHAMERICA@telit.com)  
[TS-LATINAMERICA@telit.com](mailto:TS-LATINAMERICA@telit.com)  
[TS-APAC@telit.com](mailto:TS-APAC@telit.com)

Alternatively, use:

<http://www.telit.com/en/products/technical-support-center/contact.php>

For detailed information about where to buy the Telit modules or for recommendations on accessories and components visit:

<http://www.telit.com>

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Please keep us informed of comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.





## 1.5. Text Conventions



**Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.**



**Caution or Warning – Alerts the user to important points about integrating the module. If these points are not followed, the module and end user equipment may fail or malfunction.**



**Tip or Information – Provides advice and suggestions that may be useful when integrating the module.**

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

## 1.6. Related Documents

- Digital Voice Interface Application Note, 80000NT10061A
- Product Description, 80392ST10096A
- Telit EVK2 User Guide, 1v0300704



## 2. General Product Description

### 2.1. Overview

The aim of this document is the description of typical hardware solutions useful for developing a product with the Telit DE910 module.

In this document all the basic functions of a mobile device will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace all hardware solutions and products that may be designed. Avoiding the discussed wrong solutions must be considered as mandatory. While the suggested hardware configurations must not be considered mandatory, the information given must be used as a guide and a starting point for properly developing a product with the Telit DE910 module.



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#### NOTE:

The integration of the CDMA 1xRTT/1xEV-DO Rev. A module within a user application must be done according to the design rules described in this manual.

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## 2.2. Product Specifications

DE910 Specifications	
<b>Air Interface</b>	<ul style="list-style-type: none"> <li>• CDMA 1xRTT</li> <li>• CDMA 1xEV-DO Rev. A</li> </ul>
<b>Frequency Bands</b>	<ul style="list-style-type: none"> <li>• DE910-DUAL: 800/1900MHz</li> <li>• DE910-SC: 800MHz</li> </ul>
<b>Data Service</b>	<ul style="list-style-type: none"> <li>• CDMA 1xRTT: 153.6 Kbps (full-duplex)</li> <li>• CDMA 1xEV-DO Rev. A: 3.1Mbps (F/L), 1.8Mbps (R/L)</li> </ul>
<b>Location solution</b>	gpsOne
<b>Max. RF out power</b>	<ul style="list-style-type: none"> <li>• CDMA BC0: Power class 3 (24.4dBm) for 1xRTT, Power class 3 (24dBm) for 1xEV-DO</li> <li>• CDMA BC1: Power class 2 (24.4dBm) for 1xRTT, Power class 2 (24dBm) for 1xEV-DO</li> </ul>
<b>Typical conducted sensitivity</b>	<p>a. CDMA</p> <ul style="list-style-type: none"> <li>• 1xRTT: Better than -108dBm</li> <li>• 1xEV-DO: Better than -109dBm</li> </ul> <p>b. GNSS</p> <ul style="list-style-type: none"> <li>• Acquisition sensitivity: -145dBm</li> <li>• Navigation sensitivity: -160dBm</li> <li>• Tracking sensitivity: -161dBm</li> <li>• Cold-start sensitivity: -145dBm</li> <li>• TTF: 32 sec @-130dBm</li> </ul>
<b>Device dimensions</b>	28.2mm(L) x 28.2mm(W) x 2.05mm(T)
<b>Weight</b>	3.8g
<b>Storage and Operating Temperature Range</b>	-40 ~ +85°C
<b>Normal operating voltage range</b>	3.4 ~ 4.2V
<b>IO voltage</b>	1.8V
<b>Hardware design</b>	<ul style="list-style-type: none"> <li>• RX diversity on all band</li> </ul>
<b>Interface</b>	<ul style="list-style-type: none"> <li>• 144 Land-Grid-Array interface</li> <li>• 10 general I/O ports maximum including multi-functional I/Os</li> <li>• State LED output</li> <li>• 1 A/D converter</li> <li>• 1 D/A converter (PDM output)</li> <li>• Full RS232 CMOS UART: baud rate up to 4Mbps</li> <li>• Reserved two wires CMOS UART for debugging</li> <li>• USB 2.0: baud rate up to 480Mbps</li> </ul>
<b>Antenna</b>	<ul style="list-style-type: none"> <li>• Primary antenna</li> <li>• RX Diversity antenna</li> <li>• GPS&amp;GLONASS antenna</li> </ul>



<b>Audio</b>	PCM interface for Digital audio
<b>Message</b>	SMS (MO/MT)
<b>Approvals</b>	<ul style="list-style-type: none"> <li>• Regulatory:             <ul style="list-style-type: none"> <li>- DE910-DUAL: FCC, IC</li> <li>- DE910-SC: CCC, SRRC</li> </ul> </li> <li>• Carrier: Verizon, Sprint, Aeris</li> </ul>

### 2.3. RoHS Compliance

As a part of Telit’s corporate policy of environmental protection, the DE910 complies with the RoHS (Restriction of Hazardous Substances) directive of the European Union (EU Directive 2011/65/EU).









Pin	Signal	I/O	Function	Type
M4	GND	-	Ground	
N4	GND	-	Ground	
P4	GND	-	Ground	
R4	GND	-	Ground	
N5	GND	-	Ground	
P5	GND	-	Ground	
R5	GND	-	Ground	
N6	GND	-	Ground	
P6	GND	-	Ground	
R6	GND	-	Ground	
P8	GND	-	Ground	
R8	GND	-	Ground	
P9	GND	-	Ground	
P10	GND	-	Ground	
R10	GND	-	Ground	
M12	GND	-	Ground	
B13	GND	-	Ground	
P13	GND	-	Ground	
E14	GND	-	Ground	
<b>Reserved</b>				
C1	Reserved	-	Reserved	
D1	Reserved	-	Reserved	
B2	Reserved	-	Reserved	
C2	Reserved	-	Reserved	
D2	Reserved	-	Reserved	
B3	Reserved	-	Reserved	
F3	Reserved	-	Reserved	
G3	Reserved	-	Reserved	
H3	Reserved	-	Reserved	
J3	Reserved	-	Reserved	
K3	Reserved	-	Reserved	
L3	Reserved	-	Reserved	
A4	Reserved	-	Reserved	
B4	Reserved	-	Reserved	
B5	Reserved	-	Reserved	
N7	Reserved	-	Reserved	
P7	Reserved	-	Reserved	
A8	Reserved	-	Reserved	
N8	Reserved	-	Reserved	
A9	Reserved	-	Reserved	
N9	Reserved	-	Reserved	
A10	Reserved	-	Reserved	
B10	Reserved	-	Reserved	
B11	Reserved	-	Reserved	
N10	Reserved	-	Reserved	
A11	Reserved	-	Reserved	
N11	Reserved	-	Reserved	



Pin	Signal	I/O	Function	Type
P11	Reserved	-	Reserved	
A12	Reserved	-	Reserved	
B12	Reserved	-	Reserved	
D12	Reserved	-	Reserved	
N12	Reserved	-	Reserved	
P12	Reserved	-	Reserved	
D13	Reserved	-	Reserved	
E13	Reserved	-	Reserved	
F13	Reserved	-	Reserved	
G13	Reserved	-	Reserved	
H13	Reserved	-	Reserved	
J13	Reserved	-	Reserved	
K13	Reserved	-	Reserved	
L13	Reserved	-	Reserved	
M13	Reserved	-	Reserved	
N13	Reserved	-	Reserved	
A14	Reserved	-	Reserved	
D14	Reserved	-	Reserved	
F14	Reserved	-	Reserved	
G14	Reserved	-	Reserved	
H14	Reserved	-	Reserved	
J14	Reserved	-	Reserved	
K14	Reserved	-	Reserved	
F15	Reserved	-	Reserved	
H15	Reserved	-	Reserved	
J15	Reserved	-	Reserved	



**NOTE:**

RUIM interface is reserved for Verizon/Sprint/Aeris variants and it is applicable only to RUIM variants of DE910 (DE910-SC)



**WARNING:**

Reserved pins must not be connected.



**NOTE:**

The following table is listing the main Pinout differences between the DE910 variants.

Product	BC0	BC1	GPS	Notes
DE910-DUAL	Yes	Yes	Yes	Reserved pads: A3, A5, A6, A7
DE910-SC	Yes	No	Yes	





**NOTE:**

Almost all pins not in use must be left disconnected. The only exceptions are the following pins:

PAD	Signal	
M1,M2,N1,N2,P1,P2	VBATT&VBATT_PA	
E1,G1,H1,J1,L1,A2,E2, F2,G2,H2,J2,K2,L2,R2, M3,N3,P3,R3,D4,M4,N 4,P4,R4,N5,P5,R5,N6,P 6,R6,P8,R8,P9,P10,R10, M12,B13,P13,E14	GND	
R12	ON_OFF*	
R13	HW_SHUTDOWN*	
B15	USB_D+	If not used should be connected to a Test Point
C15	USB_D-	If not used should be connected to a Test Point
A13	VBUS	If not used should be connected to a Test Point
N15	C103/TXD	If not used should be connected to a Test Point
M15	C104/RXD	If not used should be connected to a Test Point
L14	C105/RTS	If the flow control is not used it should be connected to GND
P15	C106/CTS	If not used should be connected to a Test Point
D15	TXD_AUX	If not used should be connected to a Test Point
E15	RXD_AUX	If not used should be connected to a Test Point
K1	Main Antenna	
F1	ANT_DIV (If supported by the product)	If not used it could be left unconnected, but has to be disabled by the related AT Command (AT#RXDIV): please refer to the AT User Guide for the related syntax
R9	ANT_GPS (If supported by the product)	If the GPS is not used it could be left unconnected
C3,C4,C5,C6,C7,D3,E3	Test Point	

RTS must be connected to the GND (on the module side) if flow control is not used.

The above pins are also necessary to debug the application incorporating the module.





### 3.1.1. LGA Pads Layout (DE910-DUAL)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1		ADC_IN1	RES	RES	GND	ANT_DIV	GND	GND	GND	ANTENNA	GND	VBATT	VBATT_PA	VBATT_PA		1
2	GND	RES	RES	RES	GND	GND	GND	GND	GND	GND	GND	VBATT	VBATT_PA	VBATT_PA	GND	2
3	RES	RES	TP1	TP6	TP7	RES	RES	RES	RES	RES	RES	GND	GND	GND	GND	3
4	RES	RES	TP2	GND								GND	GND	GND	GND	4
5	RES	RES	TP3									GND	GND	5		
6	RES	DVI_RX	TP4									GND	GND	6		
7	RES	DVI_TX	TP5									RES	RES	GPS_LNA_EN	7	
8	RES	DVI_CLK	GPIO_01									RES	GND	GND	8	
9	RES	DVI_WA0	GPIO_02									RES	GND	ANT_GPS	9	
10	RES	RES	GPIO_03									RES	GND	GND	10	
11	RES	RES	GPIO_04									RES	RES	VAUX/PWR MON	11	
12	RES	RES	GPIO_06	RES								GND	RES	RES	ON_OFF*	12
13	USB_VBUS	GND	GPIO_07	RES								RES	RES	RES	RES	RES
14	RES	GPIO_05	VRTC	RES	GND	RES	RES	RES	RES	RES	C105/RTS	C108/DTR	C109/DCD	C107/DSR	C125/RING	14
15		USB_D+	USB_D-	TX_AUX	RX_AUX	RES	GPIO_10	RES	RES	GPIO_08	GPIO_09	C104/RXD	C103/TXD	C106/CTS		15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Top View



**NOTE:**

The pin defined as **RES** must be considered RESERVED and not connected on any pin in the application. The related area on the application has to be kept empty.











## 4.2. Turning off the DE910 module

Turning off the device can be done in two ways:

- By software command (see DE910 Software User Guide)
- By hardware shutdown

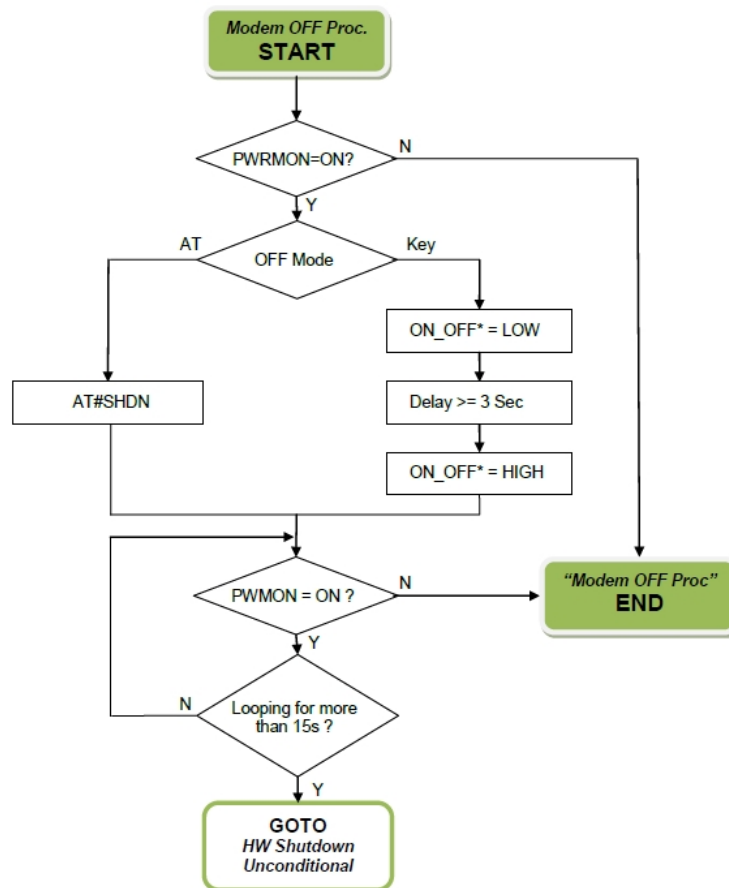
When the device is shut down by software command or by hardware shutdown, it issues a detach request to the network that informs the network that the device will no longer be reachable.



### NOTE:

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the DE910 when the module is powered OFF or during an ON/OFF transition.

The following flow chart shows the proper turnoff procedure:













**NOTE:**

Do not use any pull up resistor on the HW\_SHUTDOWN\* line or any totem pole digital output. Using a pull up resistor may bring latch up problems on the DE910 power regulator and result in improper functioning of the module. The line HW\_SHUTDOWN\* must be connected only in open collector configuration.

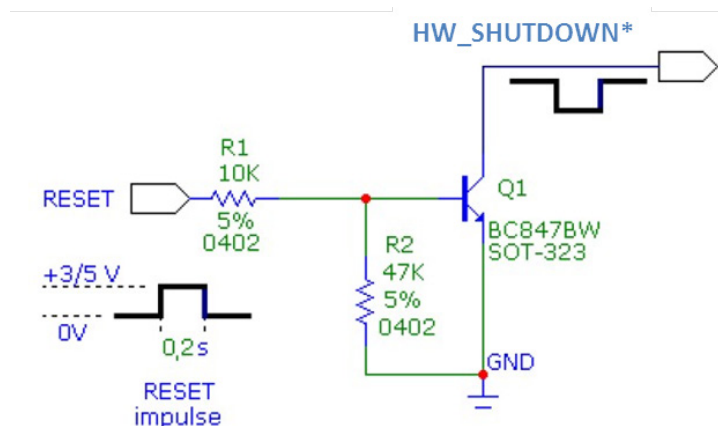


**TIP:**

The unconditional hardware Shutdown must always be implemented on the boards and the software must use it only as an emergency exit procedure.

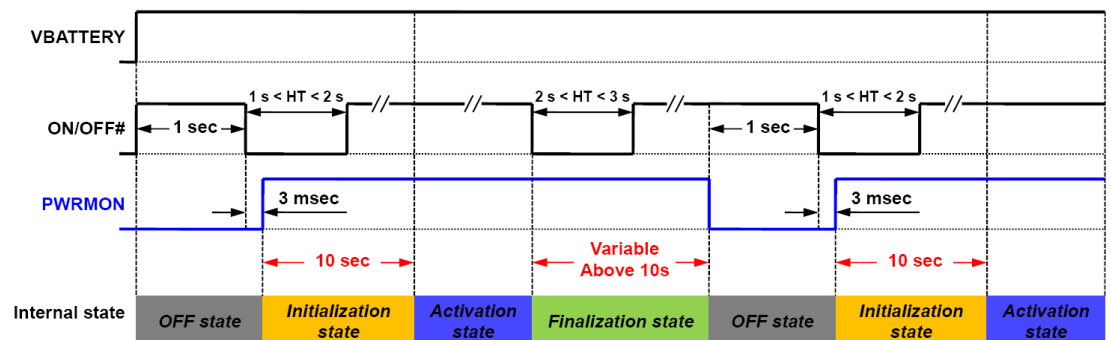
For example:

To drive the HW\_SHUTDOWN\* pad with a totem pole output of a +3/5 V microcontroller (uP\_OUT2):



## 4.4. Summary of Turning ON and OFF the Module

The chart below describes the overall sequences for turning the module ON and OFF.



## 5. Power Supply

The power supply circuitry and board layout are a very important part in the full product design and they strongly reflect on the product’s overall performance. Read carefully the requirements and the guidelines that follow for a proper design.

### 5.1. Power Supply Requirements

The external power supply must be connected to VBATT & VBATT\_PA signals and must fulfill the following requirements:

Power Supply	
Nominal Supply Voltage	3.8V
Normal Operating Voltage Range	3.4V ~ 4.2V
Extended Operating Voltage Range	3.3V ~ 4.5V




---

**NOTE:**

The Operating Voltage Range **MUST** never be exceeded. Special care must be taken when designing the application’s power supply section to avoid having an excessive voltage drop.

If the voltage drop is exceeding the limits it could cause a Power Off of the module..

Behavior in the extended operating voltage range might deviate from 3GPP2 specification.

---



Current Consumption		
Mode	Average (mA)	Mode Description
<b>Power off current (Typical)</b>		15uA(*1)
<b>Standby mode</b>		No call in progress (slot cycle index=2, hybrid mode)
AT+CFUN=1	GPS=off	<15
	GPS=on	<65
		Normal mode; full functionality of the module
AT+CFUN=4	GPS=off	<25
	GPS=on	<70
		Disabled TX and RX; modules is not registered on the network
AT+CFUN=5	GPS=off	<2.5(*2)
	GPS=on	<65
		Full functionality with power saving; Module registered on the network can receive incoming call sand SMS
<b>Tx and Rx mode</b>		A call in progress
Antenna Diversity=off	GPS=off	670
	GPS=on	735
Antenna Diversity=on	GPS=off	700
	GPS=on	705
		CDMA 1x call
Antenna Diversity=off	GPS=off	650
	GPS=on	730
Antenna Diversity=on	GPS=off	640
	GPS=on	685
		1xEV-DO call

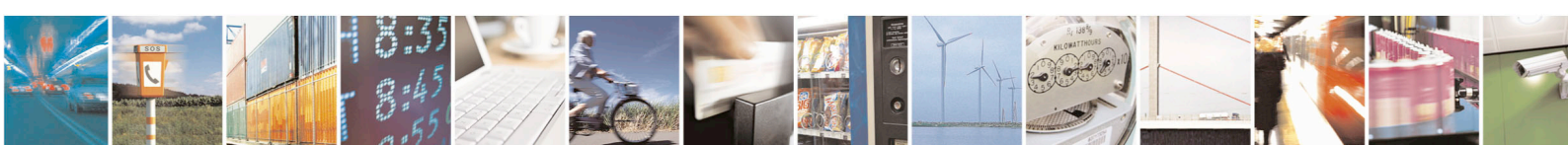
(\*1)The off current is the total supply current from the main battery with the PMIC off and the 32 kHz XTAL oscillator on.

(\*2) Standby current consumption depends on network configuration or module configuration.



**NOTE:**

The Operating Voltage Range MUST never be exceeded. Special care must be taken in order to fulfill min/max supply voltage requirement.



**TIP:**

The electrical design for the power supply should be made ensuring it will be capable of a peak current output of at least 1A.

## 5.2. General Design Rules

The principal guidelines for the Power Supply Design embrace three different design steps:

- the electrical design
- the thermal design
- the PCB layout

### 5.2.1. Electrical Design Guidelines

The electrical design of the power supply depends strongly on the power source where this power is drained. We will distinguish them into three categories:

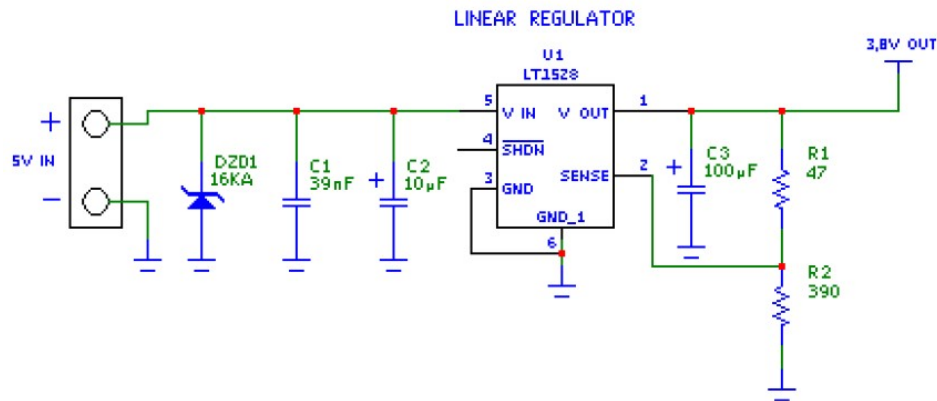
- +5V input (typically PC internal regulator output)
- +12V input (typically automotive)
- Battery

### 5.2.2. + 5V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence there is not a big difference between the input source and the desired output so a linear regulator can be used. A switching power supply will not be suitable because of the low drop-out requirements.
- When using a linear regulator, a proper heat sink must be provided in order to dissipate the power generated.
- A Bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks close to the DE910. A 100 $\mu$ F tantalum capacitor is usually suited.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- A protection diode must be inserted close to the power input in order to save the DE910 from power polarity inversion.



An example of a linear regulator with 5V input:



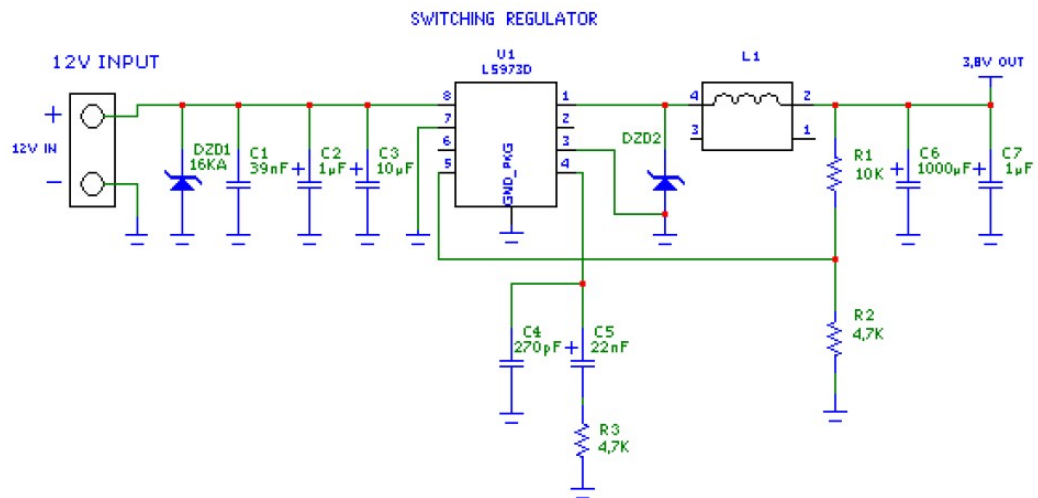
### 5.2.3. +12V Input Source Power Supply Design Guidelines

- The desired output for the power supply is 3.8V, hence due to the big difference between the input source and the desired output, a linear regulator is not suitable and must not be used. A switching power supply would be preferable because of its better efficiency, especially with the 1A peak current load represented by DE910.
- When using a switching regulator, a 500 kHz or more switching frequency regulator is preferable because of its smaller inductor size and its faster transient response. This allows the regulator to respond quickly to the current peaks absorption.
- In any case, the frequency and switching design selection is related to the application to be developed due to the fact the switching frequency could also generate EMC interferences.
- For car PB battery the input voltage can rise up to 15.8V and this must be kept in mind when choosing components: all components in the power supply must withstand this voltage.
- A bypass low ESR capacitor of adequate capacity must be provided in order to cut the current absorption peaks. A 100µF tantalum capacitor is usually suited for this.
- Make sure the low ESR capacitor on the power supply output (usually a tantalum one) is rated at least 10V.
- For car applications a spike protection diode must be inserted close to the power input in order to clean the supply from spikes.
- A protection diode must be inserted close to the power input in order to save the DE910 from power polarity inversion. This can be the same diode as for spike protection.





An example of switching regulator with 12V input is in the schematic below:



### 5.2.4. Battery Source Power Supply Design Guidelines

The desired nominal output for the power supply is 3.8V and the maximum voltage allowed is 4.2V. A single 3.7V lithium-ion cell battery type is ideal to supply power to the Telit DE910 module.



#### WARNING:

The three battery cells (Ni/Cd or Ni/MH 3.6V nom. battery types or 4V PB types) MUST NOT be used directly because their maximum voltage can rise over the absolute maximum voltage for the DE910 and cause damage. USE only Li-Ion battery types.

- A bypass low (usually a 100uF tantalum) ESR capacitor with adequate capacity must be provided in order to cut the current absorption peaks.
- Make sure the low ESR capacitor (usually a tantalum) is rated at least 10V.
- A protection diode must be inserted close to the power input in order to protect the DE910 module from power polarity inversions when connecting the battery.
- The battery capacity must be at least 500mAh in order to withstand the current peaks of 1A. The suggested battery capacity is from 500mAh to 1000mAh.

### 5.2.5. Thermal Design Guidelines

The thermal design for the power supply heat sink must be done with the following specifications:

- Average current consumption during CDMA 1x / 1xEV-DO transmission @PWR level max : 750 mA
- Average GPS current during GPS ON (Power Saving disabled) in DE910 : 55 mA







**NOTE:**

The average consumption during transmissions depends on the power level at which the device is requested to transmit via the network. The average current consumption hence varies significantly.

Considering the very low current during idle, especially if the Power Saving function is enabled, it is possible to consider from the thermal point of view that the device absorbs current significantly only during calls.

If we assume that the device stays in transmission for short periods of time (a few minutes) and then remains for quite a long time in idle (one hour), then the power supply always has time to cool down between the calls and the heat sink could be smaller than the calculated for 750mA maximum RMS current. There could even be a simple chip package (no heat sink).

Moreover in average network conditions the device is requested to transmit at a lower power level than the maximum and hence the current consumption will be less than 750mA (usually around 250 mA).

For these reasons the thermal design is rarely a concern and the simple ground plane where the power supply chip is placed can be enough to ensure a good thermal condition and avoid overheating.

The heat generated by the DE910 must be taken into consideration during transmission at 24.4dBm max during calls. This generated heat will be mostly conducted to the ground plane under the DE910. The application must be able to dissipate heat.

In the CDMA 1x/1xEV-DO mode, since DE910 emits RF signals continuously during transmission, special attention must be paid to how to dissipate the heat generated.

The current consumption will be up to about 750mA in CDMA 1x continuously at the maximum TX output power (24.4dBm). Thus, you must arrange the area on the application PCB must be as large as possible under DE910.

The DE910 must be mounted on the large ground area of the application board and make many ground vias to dissipate the heat.

### 5.2.6. Power Supply PCB layout Guidelines

As seen in the electrical design guidelines, the power supply must have a low ESR capacitor on the output to cut the current peaks and a protection diode on the input to protect the supply from spikes and polarity inversion. The placement of these components is crucial for the correct operation of the circuitry. A misplaced component can be useless or can even decrease the power supply performance.

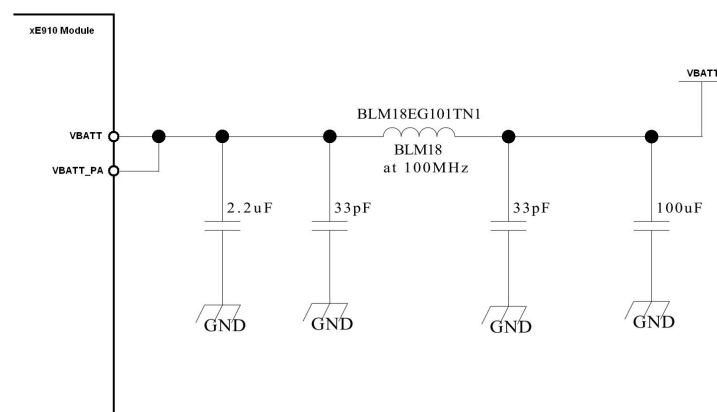
- The bypass low ESR capacitor must be placed close to the Telit DE910 power input pads, or if the power supply is a switching type, the capacitor can be placed close to the inductor to cut the ripple if the PCB trace from the capacitor to DE910 is wide enough to ensure a drop-less connection even during the 1A current peaks.



- The protection diode must be placed close to the input connector where the power source is drained.
- The PCB traces from the input connector to the power regulator IC must be wide enough to ensure no voltage drops occur when the 1A current peaks are absorbed. While a voltage drop of hundreds of mV may be acceptable from the power loss point of view, the same voltage drop may not be acceptable from the noise point of view. If the application does not have an audio interface but only uses the data feature of the Telit DE910, then this noise is not as disruptive and the power supply layout design can be more forgiving.
- The PCB traces to DE910 and the Bypass capacitor must be wide enough to ensure no significant voltage drops occur when the 1A current peaks are absorbed. This is a must for the same above-mentioned reasons. Try to keep this trace as short as possible.
- The PCB traces connecting the switching output to the inductor and the switching diode must be kept as short as possible by placing the inductor and the diode very close to the power switching IC (only for switching power supply). This is done in order to reduce the radiated field (noise) at the switching frequency (usually 100-500 kHz).
- The use of a good common ground plane is suggested.
- The placement of the power supply on the board must be done in a way to guarantee that the high current return paths in the ground plane are not overlapped with any noise sensitive circuitry such as the microphone amplifier/buffer or earphone amplifier.
- The power supply input cables must be kept separate from noise sensitive lines such as microphone/earphone cables.
- The insertion of EMI filter on VBATT pins is suggested in those designs where antenna is placed close to battery or supply lines.

A ferrite bead like Murata BLM18EG101TN1 or Taiyo Yuden P/N FBMH1608HM101 can be used for this purpose.

The below figure shows the recommended circuit:









- If EM noisy devices are present on the PCB hosting the DE910, such as fast switching ICs, take care of shielding them with a metal frame cover.
- If EM noisy devices are not present around the line, use of geometries like Micro strip or Grounded Coplanar Waveguide are preferred since they typically ensure less attenuation when compared to a Strip line having same length.

## 6.1.2. PCB Guidelines in case of FCC certification

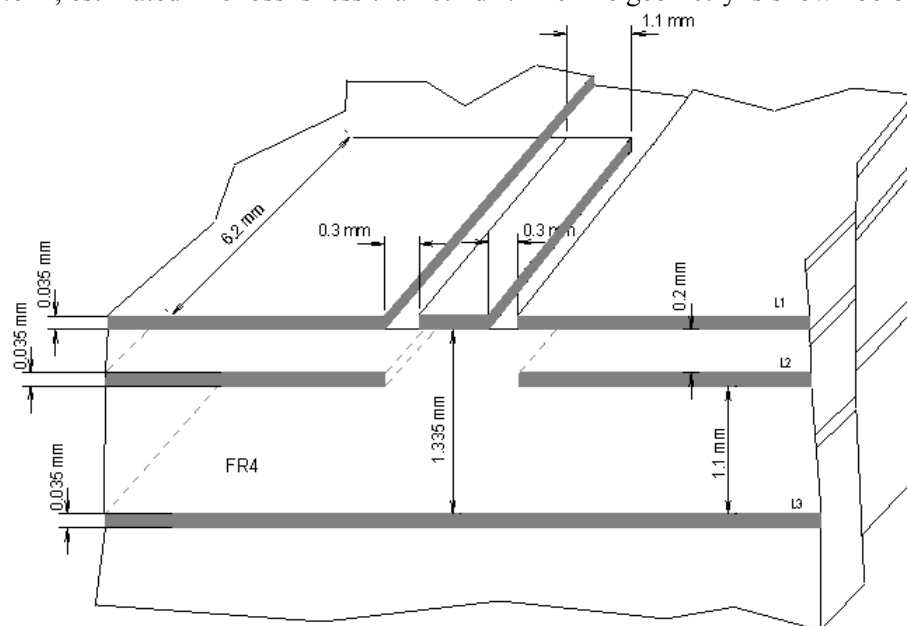
In the case FCC certification is required for an application using DE910-DUAL, according to FCC KDB 996369 for modular approval requirements, the transmission line has to be similar to that implemented on module's interface board and described in the following chapter.

### 6.1.2.1.1. Transmission line design

During the design of the DE910 interface board, the placement of components has been chosen properly, in order to keep the line length as short as possible, thus leading to lowest power losses possible. A Grounded Coplanar Waveguide (G-CPW) line has been chosen, since this kind of transmission line ensures good impedance control and can be implemented in an outer PCB layer as needed in this case. A SMA female connector has been used to feed the line.

The interface board is realized on a FR4, 4-layers PCB. Substrate material is characterized by relative permittivity  $\epsilon_r = 4.6 \pm 0.4 @ 1 \text{ GHz}$ ,  $\text{TanD} = 0.019 \div 0.026 @ 1 \text{ GHz}$ .

A characteristic impedance of nearly  $50 \Omega$  is achieved using trace width = 1.1 mm, clearance from coplanar ground plane = 0.3 mm each side. The line uses reference ground plane on layer 3, while copper is removed from layer 2 underneath the line. Height of trace above ground plane is 1.335 mm. Calculated characteristic impedance is  $51.6 \Omega$ , estimated line loss is less than 0.1 dB. The line geometry is shown below:

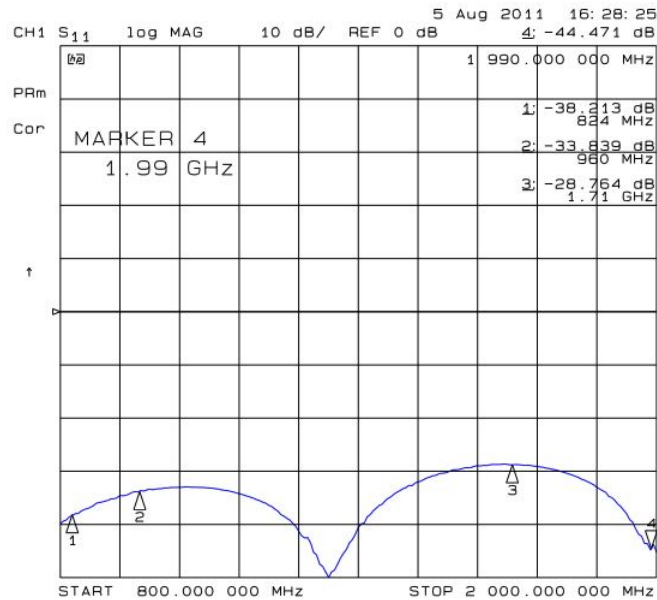




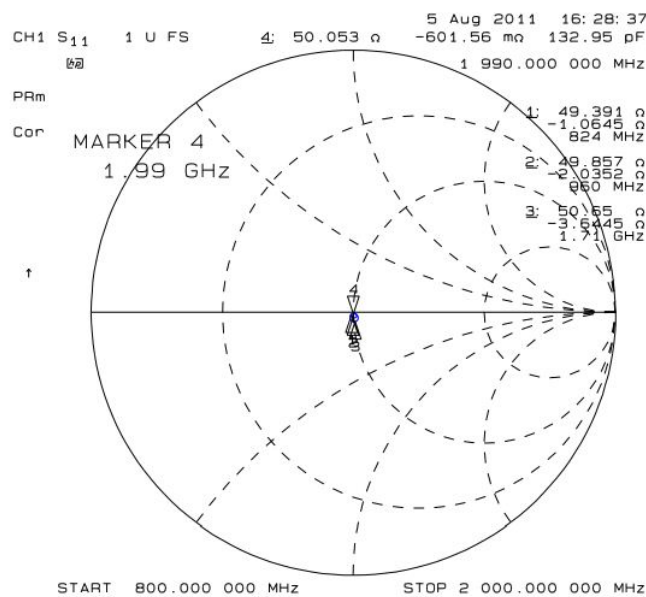
### 6.1.2.1.1.2. Transmission line measurements

HP8753E VNA (Full-2-port calibration) has been used in this measurement session. A calibrated coaxial cable has been soldered at the pad corresponding to RF output; a SMA connector has been soldered to the board in order to characterize the losses of the transmission line including the connector itself. During Return Loss / impedance measurements, the transmission line has been terminated to 50  $\Omega$  load.

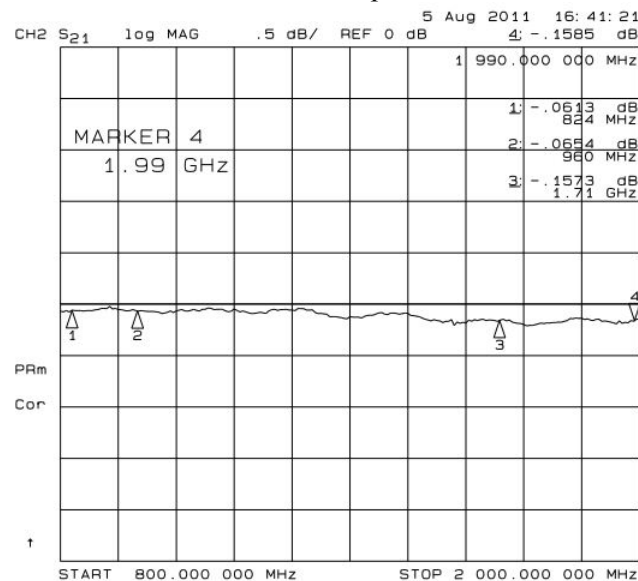
Return Loss plot of line under test is shown below:



Line input impedance (in Smith Chart format, once the line has been terminated to 50  $\Omega$  load) is shown in the following figure:



Insertion Loss of G-CPW line plus SMA connector is shown below:



### 6.1.3. CDMA Antenna – Installation Guidelines

- Install the antenna in a place covered by the CDMA signal.
- If the device antenna in the application is located greater than 20cm from the human body and there are no co-located transmitters then the Telit FCC/IC approvals can be re-used by the end product.
- Antenna shall not be installed inside metal cases.
- Antenna shall be installed also according antenna manufacture instructions.



#### WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect DE910 or customer specific requirements from ESD event to Antenna port (K1).



## 6.2. Antenna Diversity Requirements

This product includes an input for a second RX antenna to improve the radio sensitivity. The function is called Antenna Diversity.

CDMA Antenna Diversity Requirements	
<b>Frequency range</b>	Depending frequency band(s) provided by the network operator, the customer must use the most suitable antenna for that/those band(s)
<b>Bandwidth</b>	70 MHz in CDMA BC0 140 MHz in CDMA BC1
<b>Impedance</b>	50 Ohm

When using the Telit DE910, since there's no antenna connector on the module, the antenna must be connected to the DE910 antenna pad (F1) by means of a transmission line implemented on the PCB.

In the case that the antenna is not directly connected at the antenna pad of DE910, then a PCB line is required.



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### NOTE:

If the RX Diversity is not used/connected, disable the Diversity functionality using the AT#CRXD command and leave the pad F1 unconnected. Please refer to the AT command User Guide in detail.

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### WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect DE910 or customer specific requirements from ESD event to Antenna port (F1).

---



## 6.3. GNSS Antenna Requirements

The use of an active GNSS antenna is required to achieve better performance.

The module is provided with a Digital Output signal to enable the external LNA (pad R7).

Parameter	Min	Max
Output high level	1.35V	1.8V
Output low level	0.0V	0.45V

### 6.3.1. Combined GNSS Antenna

The use of combined CDMA/GNSS antenna is not recommended. This solution could generate extremely poor GNSS reception and also the combined antenna requires an additional diplexer and adds a loss in the RF route.

### 6.3.2. Linear and Patch GNSS Antenna

Using this type of antenna introduces at least 3dB of loss if compared to a circularly polarized (CP) antenna. Having a spherical gain response instead of a hemispherical gain response could aggravate the multipath behaviour & create poor position accuracy.

### 6.3.3. The Design Considerations to enhanced GNSS performance

Depending on the characteristics and requirements unique to the customer's designs, the use of an external LNA or an external active antenna may be required to achieve best performance.

The optional external LNA should be dimensioned to avoid an excessive LNA gain that can introduce jamming, spurious, degrade IIP3, and saturate the receiver.

The configurations of an external device must fulfill the following requirements:

- An external passive antenna (GPS only)
- An external active antenna (GPS or GNSS)
- An external passive antenna, GNSS pre-Filter , and GNSS LNA (GPS or GNSS)





**NOTE:**

The external GNSS LNA and GNSS pre-Filter shall be required for GLONASS application. GNSS LNA requirement shall fulfill the following specifications.

- Frequency = 1565 ~ 1606MHz
- Power Gain  $|S_{21}|^2 = 14 \sim 17\text{dB}$
- NF < 1dB

GNSS pre-Filter requirement shall fulfill the following requirements.

- Source and Load Impedance = 50Ohm
- Insertion Loss (1575.42 ~ 1576.42MHz) = 1.4dB (Max)
- Insertion Loss (1565.42 ~ 1585.42MHz) = 2.0dB (Max)
- Insertion Loss (1597.5515 ~ 1605.886MHZ) = 2.0dB (Max)

The external active antenna for the Telit DE910 device must fulfill the following requirements:

GNSS Antenna Requirements	
<b>Frequency range</b>	1575.42MHz (GPS L1) 1597.55 ~ 1605.89MHz (GLONASS)
<b>Bandwidth</b>	$\pm 1.023\text{MHz}$ (GPS L1) 8.34MHz (GLONASS)
<b>Impedance</b>	50 Ohm
<b>LNA NF</b>	< 1dB
<b>LNA Gain</b>	14 ~ 17dB
<b>LNA Input Voltage</b>	3.0V or 5.0V



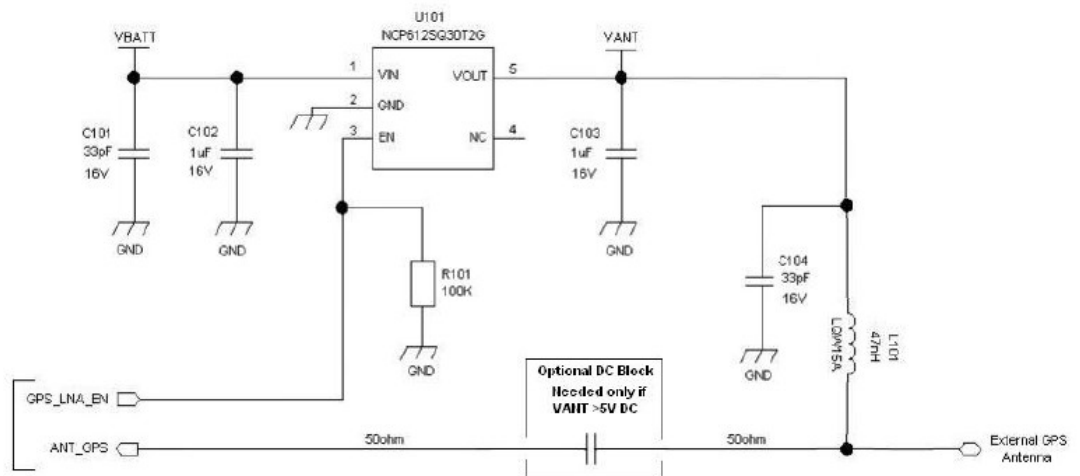
**NOTE:**

The maximum DC voltage applicable to ANT\_GPS pin is 5V. In case this is exceeded, a series capacitor has to be included in the design to avoid exceeding the maximum input DC level.





An example of GNSS antenna supply circuit is shown in the following image:



When using the Telit DE910, since there's no antenna connector on the module, the antenna must be connected to the DE910 through the PCB with the antenna pad.

In the case that the antenna is not directly connected at the antenna pad of the DE910, then a PCB line is required.

This line of transmission shall fulfill the following requirements:

Antenna Line on PCB Requirements	
<b>Characteristic Impedance</b>	50Ohm
<b>Max Attenuation</b>	0.3dB
Coupling with other signals shall be avoided	
Cold End (Ground Plane) of antenna shall be equipotential to the DE910 ground pads	

Furthermore if the device is developed for the US and/or Canada market, it must comply with the FCC and/or IC requirements.

This device is to be used only for mobile and fixed application.



**WARNING:**

The DE910 software is implemented differently depending on the configurations of an external device. Please refer to the AT command User Guide in detail.



### 6.3.4. GNSS Antenna – PCB Line Guidelines

- Ensure that the antenna line impedance is 50ohm.
- Keep line on the PCB as short as possible to reduce the loss.
- Antenna line must have uniform characteristics, constant cross section, avoid meanders and abrupt curves.
- Keep one layer of the PCB used only for the Ground plane; if possible.
- Surround (on the sides, over and under) the antenna line on PCB with Ground. Avoid having other signal tracks directly facing the antenna line track.
- The Ground around the antenna line on PCB has to be strictly connected to the main Ground plane by placing vias once per 2mm at least.
- Place EM noisy devices as far as possible from DE910 antenna line.
- Keep the antenna line far away from the DE910 power supply lines.
- If EM noisy devices are around the PCB hosting the DE910, such as fast switching ICs, take care of shielding of antenna line by burying it inside the layers of PCB and surround it with Ground planes; or shield it with a metal frame cover.
- If you do not have EM noisy devices around the PCB of DE910, use a strip line on the superficial copper layer for the antenna line. The line attenuation will be lower than a buried one.

### 6.3.5. GNSS Antenna – Installation Guidelines

- The DE910, due to its sensitivity characteristics, is capable of performing a fix inside buildings. However, the sensitivity could be affected by the building characteristics i.e. shielding.
- The Antenna must not be co-located or operating in conjunction with any other antenna or transmitter.
- Antenna shall not be installed inside metal cases.
- Antenna shall be installed also according antenna manufacture instructions.



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#### **WARNING:**

Consider a mechanical design and a low-capacitance ESD protection device to protect DE910 or customer specific requirements from ESD event to GPS port (R9).

---

## 7. USB Port

The DE910 module includes a Universal Serial Bus (USB) transceiver, which operates at USB high-speed (480Mbits/sec).

It is compliant with the USB 2.0 specification and can be used for diagnostic monitoring, control and data transfers.

The table below describes the USB interface signals:

Pin	Signal	I/O	Function	Type
B15	USB_D+	I/O	USB differential Data(+)	
C15	USB_D-	I/O	USB differential Data(-)	
A13	VBUS	I	Power sense for the internal USB transceiver	5V

The USB\_DPLUS and USB\_DMINUS signals have a clock rate of 480MHz. The signal traces should be routed carefully. Trace lengths, number of vias and capacitive loading should be minimized. The impedance value should be as close as possible to 90 Ohms differential.




---

### WARNING:

Consider a mechanical design and a low-capacitance ESD protection device to protect DE910 or customer specific requirements from ESD event to USB lines (B15, C15 and A13).

---



## 8. Serial Port

The serial ports on the Telit DE910 are the interface between the module and OEM hardware.

2 serial ports are available on the module:

- Modem Serial Port 1 (Main)
- Modem Serial Port 2 (Auxiliary)

Several configurations can be designed for the serial port on the OEM hardware.

The most common are:

- RS232 PC comport
- Microcontroller UART@1.8V(Universal Asynchronous Receiver Transmit)
- Microcontroller UART@5V or other voltages different from 1.8V

Depending on the type of serial port on the OEM hardware, a level translator circuit may be needed to make the system work.

Serial port 1 is a +1.8V UART with all the 7 RS232 signals.

Serial port 2 is a +1.8V Auxiliary UART.

The electrical characteristics of the serial port are explained in the following tables:

### Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on non-power pin with respect to ground	-0.3	+2.3V

### Operating Range - Interface levels

Parameter	Min	Max
Input high level	1.5V	2.1 V
Input low level	-0.3V	0.35V
Output high level	1.35V	1.8V
Output low level	0V	0.45V



## 8.1. Modem Serial Port 1

Serial port 1 on the DE910 is a +1.8V UART with all 7 RS232 signals.

It differs from the PC-RS232 in the signal polarity (RS232 is reversed) and levels.

Pin	Signal	I/O	Function	Type
N14	DCD	O	Data Carrier Detect	1.8V
M15	RXD	O	Transmit line *see Note	1.8V
N15	TXD	I	Receive line *see Note	1.8V
M14	DTR	I	Data Terminal Ready	1.8V
P14	DSR	O	Data Set Ready	1.8V
L14	RTS	I	Request to Send	1.8V
P15	CTS	O	Clear to Send	1.8V
R14	RI	O	Ring Indicator	1.8V

The following table shows the typical input value(pulled inside the baseband chipset) and status for input lines all module states:

Signal/State	OFF	RESET	ON	Powersaving	PU tied to
TXD	unknown	PD: 21K~210K	PU: 39K~390K	PU: 39K~390K	1.8V
RTS		PD: 21K~210K			
DTR		PU: 39K~390K			



**NOTE:**

For minimum implementation, only the TXD and RXD lines must be connected, the other lines can be left open provided a software flow control is implemented.



**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the DE910 when the module is powered off or during an ON/OFF transition.







**NOTE:**

According to V.24, RX/TX signal names are referred to the application side. Therefore, on the DE910 side these signals are in the opposite direction: TXD on the application side will be connected to the receive line (here named TXD/ rx\_uart ) of the DE910 serial port and vice versa for RX.



**NOTE:**

High-speed UART supports up to 4Mbps. Please refer to the AT command User Guide in detail.



**WARNING:**

Consider a mechanical design and a low-capacitance ESD protection device to protect DE910 or customer specific requirements from ESD event to UART port (M15, N15, P15 and L14).

## 8.2. Modem Serial Port 2

Serial port 2 on the DE910 is a +1.8V UART with only the RX and TX signals.

The signals of the DE910 serial port are:

Pin	Signal	I/O	Function	Type
D15	TX_AUX	O	Auxillary UART (TX Data to DTE)	1.8V
E15	RX_AUX	I	Auxillary UART (RX Data from DTE)	1.8V



**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the DE910 when the module is powered off or during an ON/OFF transition.

## 8.3. RS232 Level Translation

In order to interface the Telit DE910 with a PC com port or a RS232 (EIA/TIA-232) application, a level translator is required. This level translator must:

- Invert the electrical signal in both directions
- Change the level from 0/1.8V to +/-15V



Actually, the RS232 UART 16450, 16550, 16650 & 16750 chipsets accept signals with lower levels on the RS232 side (EIA/TIA-562), allowing a lower voltage-multiplying ratio on the level translator. Note that the negative signal voltage must be less than 0V and hence some sort of level translation is always required.

The simplest way to translate the levels and invert the signal is by using a single chip level translator. There are a multitude of them, differing in the number of drivers and receivers and in the levels (be sure to get a true RS232 level translator not a RS485 or other standards).

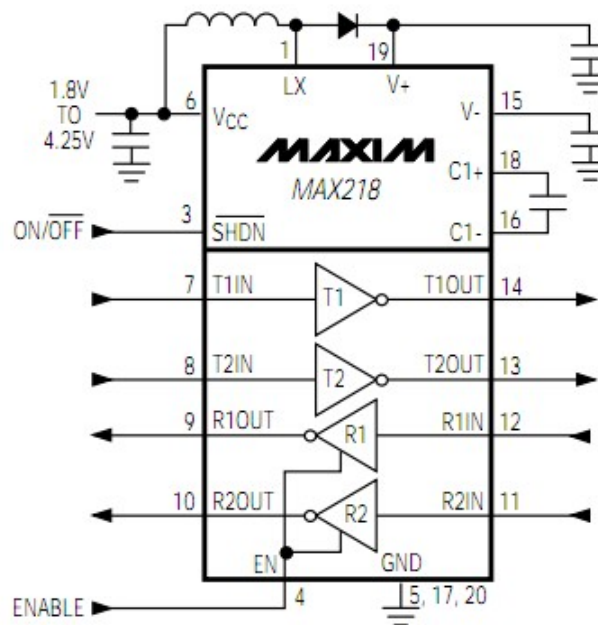
By convention the driver is the level translator from the 0-1.8V UART to the RS232 level. The receiver is the translator from the RS232 level to 0-1.8V UART.

In order to translate the whole set of control lines of the UART you will need:

- 5 drivers
- 3 receivers

An example of RS232 level adaption circuitry could be accomplished using a MAXIM transceiver (MAX218).

In this case the chipset is capable of translating directly from 1.8V to the RS232 levels (Example on 4 signals only).

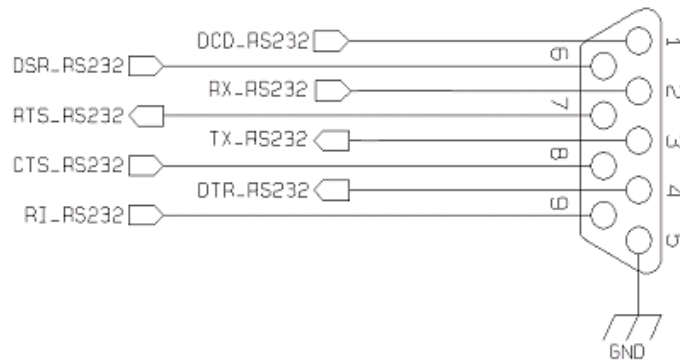


**NOTE:**

In this case the length of the lines on the application has to be taken into account to avoid problems in case of High-speed rates on RS232.



The RS232 serial port lines are usually connected to a DB9 connector with the following layout:



## 9. Audio Section Overview

The DE910 module doesn't support an analog audio interface and supports one Digital Audio bus.

In order to develop an application including an Analog Audio it is necessary to add a dedicated CODEC on the Application design.

For further information, please refer to the “Digital Voice Interface Application Note”.

### 9.1. Electrical Characteristics

The product is providing one Digital Audio Interface (DVI) on the following Pins:

Pin	Signal	I/O	Function	Type
B9	DVI_WA0	I/O	Digital Voice interface (WA0)	1.8V
B6	DVI_RX	I	Digital Voice interface (RX)	
B7	DVI_TX	O	Digital Voice interface (TX)	
B8	DVI_CLK	I/O	Digital Voice interface (CLK)	

#### 9.1.1. CODEC Example

Please refer to the Digital Voice Interface Application note.



## 10. General Purpose I/O

The general-purpose I/O pads can be configured to act in three different ways:

- Input
- Output
- Alternate function (internally controlled)

Input pads can only be read and report the digital value (high or low) present on the pad at the read time.

Output pads can only be written to set the value of the pad or queried.

An alternate function pad is internally controlled by the DE910 firmware and acts depending on the function implemented.

The following GPIOs are available on the DE910.

Pin	Signal	I/O	Function	Drive Strength	Type
C8	GPIO_01	I/O	Configurable GPIO	2 mA	1.8V
C9	GPIO_02	I/O	Configurable GPIO	2 mA	1.8V
C10	GPIO_03	I/O	Configurable GPIO	2 mA	1.8V
C11	GPIO_04	I/O	Configurable GPIO	2 mA	1.8V
B14	GPIO_05	I/O	Configurable GPIO	2 mA	1.8V
C12	GPIO_06	I/O	Configurable GPIO	2 mA	1.8V
C13	GPIO_07	I/O	Configurable GPIO	2 mA	1.8V
K15	GPIO_08	I/O	Configurable GPIO	2 mA	1.8V
L15	GPIO_09	I/O	Configurable GPIO	2 mA	1.8V
G15	GPIO_10	I/O	Configurable GPIO	2 mA	1.8V





## 10.1. Logic Level Specification

Where not specifically stated, all the interface circuits work at 1.8V CMOS logic levels.

The following table shows the logic level specifications used in the DE910 interface circuits:

### Absolute Maximum Ratings -Not Functional

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.3V

### Operating Range - Interface levels (1.8V CMOS)

Parameter	Min	Max
Input high level	1.5V	2.1V
Input low level	0.0V	0.35V
Output high level	1.35V	1.8V
Output low level	0.0V	0.45V

### Current characteristics

Parameter	Typical
Output Current	2mA
Input Current	30uA

## 10.2. Using a GPIO Pad as Input

The GPIO pads, when used as inputs, can be connected to a digital output of another device and report its status, provided this device has interface levels compatible with the 1.8V CMOS levels of the GPIO.

If the digital output of the device is connected with the GPIO input, the pad has interface levels different from the 1.8V CMOS. It can be buffered with an open collector transistor with a 4.7KΩ pull-up resistor to 1.8V.



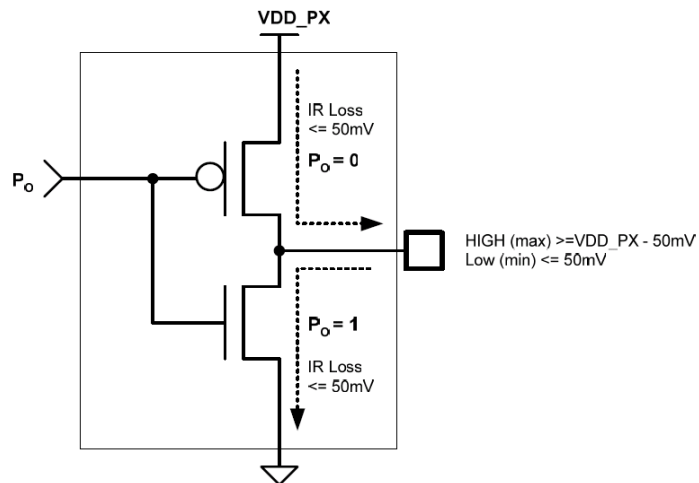


**NOTE:**

In order to avoid a back powering effect it is recommended to avoid having any HIGH logic level signal applied to the digital pins of the module when it is powered OFF or during an ON/OFF transition.

### 10.3. Using a GPIO Pad as Output

The GPIO pads, when used as outputs, can drive 1.8V CMOS digital devices or compatible hardware. When set as outputs, the pads have a push-pull output and therefore the pull-up resistor may be omitted.



output PAD equivalent circuit

### 10.4. Using the Temperature Monitor Function

#### 10.4.1. Short Description

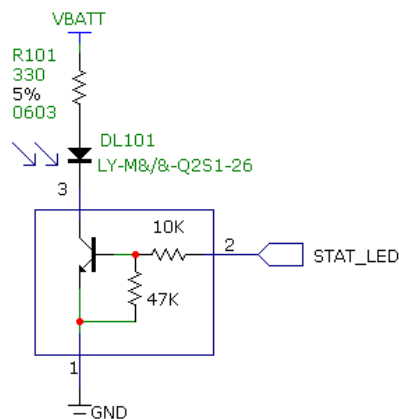
The Temperature Monitor is a function of the module that permits control of its internal temperature and if properly set (see the #TEMPMON command on AT Interface guide) raises to High Logic level a GPIO when the maximum temperature is reached.



## 10.5. Indication of Network Service Availability

The STAT\_LED pin status shows information on the network service availability and Call status. In the DE910 modules, the STAT\_LED usually needs an external transistor to drive an external LED. Because of the above, the status indicated in the following table is reversed with respect to the pin status:

LED status	Device Status
Permanently off	Device off
Fast blinking (Period 1s, Ton 0,5s)	Net search / Not registered / turning off
Slow blinking (Period 3s, Ton 0,3s)	Registered full service
Permanently on	a call is active



## 10.6. RTC Bypass Output

The VRTC pin brings out the Real Time Clock supply, which is separate from the rest of the digital part, allowing only RTC to be active when all the other parts of the device are off. To this power output a backup capacitor can be added in order to increase the RTC autonomy during power off of the battery. No devices must be powered from this pin.

For additional details on the Backup solutions please refer to the related application note (xE910 RTC Backup Application Note).

VRTC also supplies reference power to help DE910 check the time from SMPL (Sudden Momentary Power Loss).

So it is recommended as best practice to connect VRTC to a shunt capacitor (VRTC to GND) and the acceptable capacitor value is:

Parameter	Min
Keep-alive capacitor on Pad no. = C14	6.8uF



**NOTE:**

VBATT must be supplied in order to use RTC function.



**NOTE:**

It is recommended to add a keep-alive capacitor on VRTC.



**WARNING:**

NO devices must be powered from this pin.



## 10.7. VAUX/PWRMON Power Output

A regulated power supply output is provided in order to supply small devices from the module. This output is active when the module is ON and goes OFF when the module is shut down. The operating range characteristics of the supply are:

### Operating Range – VAUX/PWRMON power supply

Parameter	Min	Typical	Max
Output voltage	1.77V	1.8V	1.83V
Output current			200mA
Output bypass capacitor (Inside the module)		2.2 $\mu$ F	









## 12. Test Point

These pins are needed in order to analyze DE910 on the application board.

The signals of the DE910 are:

PAD	Signal	I/O	Function	Type
C3	TP1		Test Point	TP
C4	TP2		Test Point	TP
C5	TP3		Test Point	TP
C6	TP4		Test Point	TP
C7	TP5		Test Point	TP
D3	TP6		Test Point	TP
E3	TP7		Test Point	TP

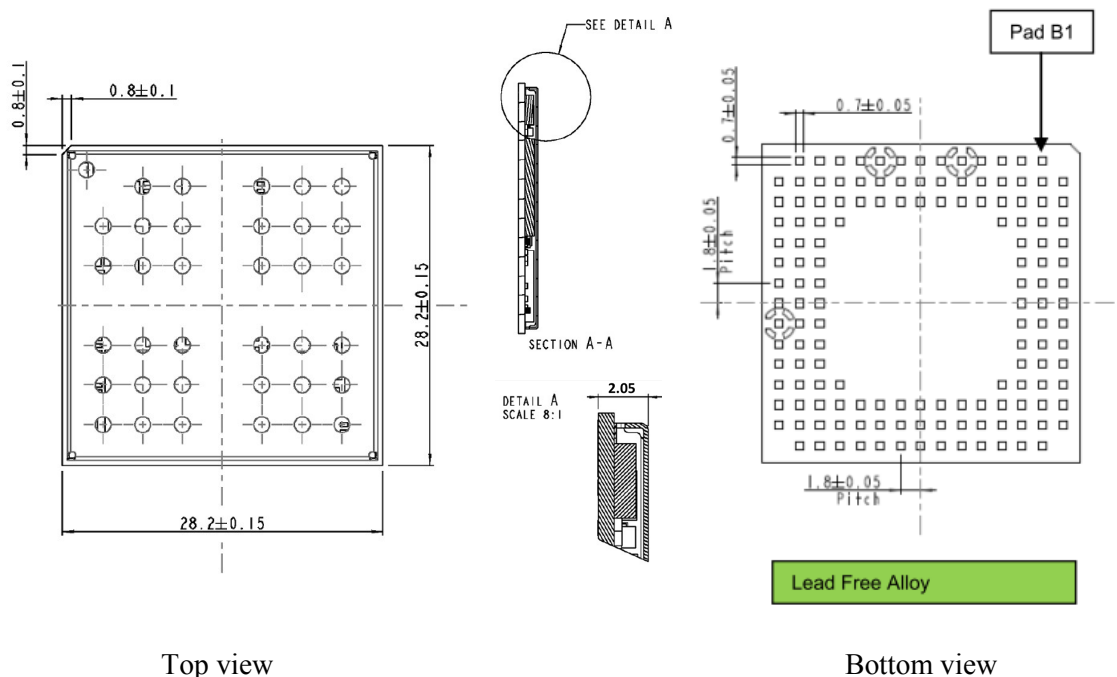


## 13. Mounting the Module on your Board

### 13.1. General

The DE910 has been designed in order to be compliant with a standard lead-free SMT process.

### 13.2. Module Finishing & Dimensions



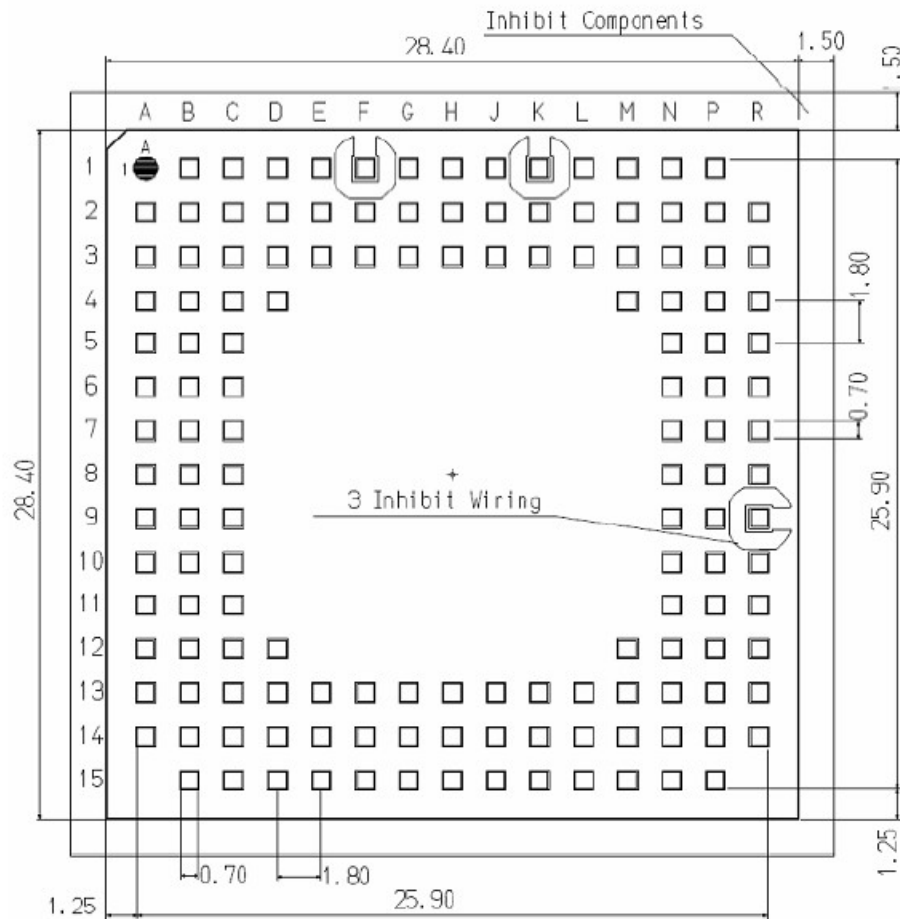
Top view

Bottom view

(Dimensions in mm)



### 13.3. Recommended foot print for the application



144 pins

< Top View >

In order to easily rework the DE910 it is suggested to consider having a 1.5 mm placement inhibit area around the module on the application.

It is also suggested, as a common rule for an SMT component, to avoid having a mechanical part of the application in direct contact with the module.



**NOTE:**

In the customer application, the region under WIRING INHIBIT (see figure) must be clear from signal or ground paths.



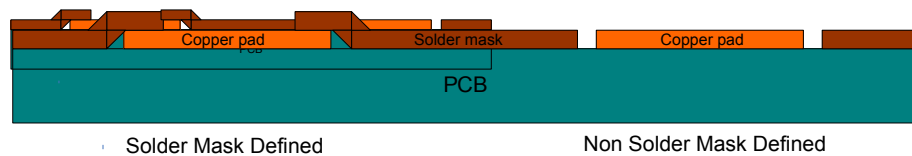


### 13.4. Stencil

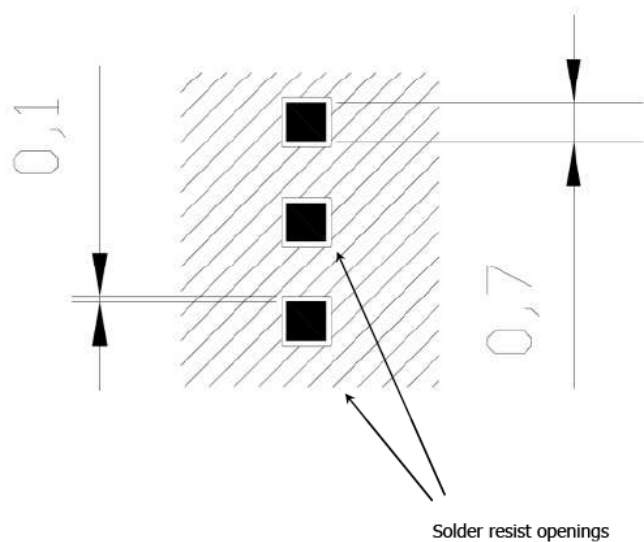
Stencil's apertures layout can be the same as the recommended footprint (1:1). we suggest a thickness of stencil foil  $\geq 120 \mu\text{m}$ .

### 13.5. PCB Pad Design

Non solder mask defined (NSMD) type is recommended for the solder pads on the PCB.

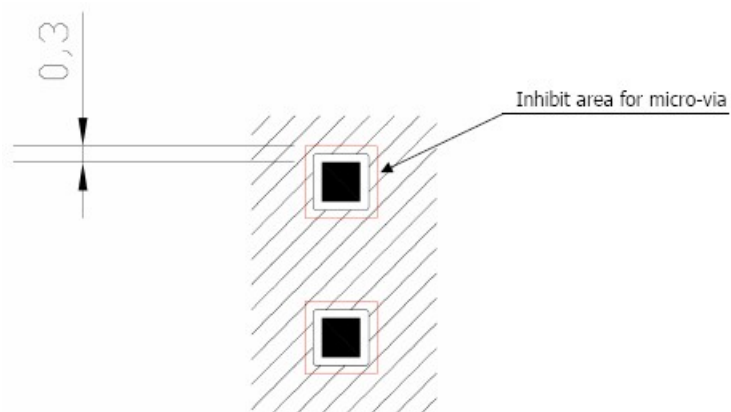


### 13.6. Recommendations for PCB Pad Dimensions (mm)



It is not recommended to place via or micro-via not covered by solder resist in an area of 0.3 mm around the pads unless it carries the same signal as the pad itself (see following figure).





Holes in pad are allowed only for blind holes and not for through holes.

Recommendations for PCB Pad Surfaces:

Finish	Layer thickness (um)	Properties
Electro-less Ni / Immersion Au	3 ~ 7 / 0.05 ~ 0.15	good solder ability protection, high shear force values

The PCB must be able to resist the higher temperatures which are occurring at the lead-free process. This issue should be discussed with the PCB-supplier. Generally, the wettability of tin-lead solder paste on the described surface plating is better compared to lead-free solder paste.



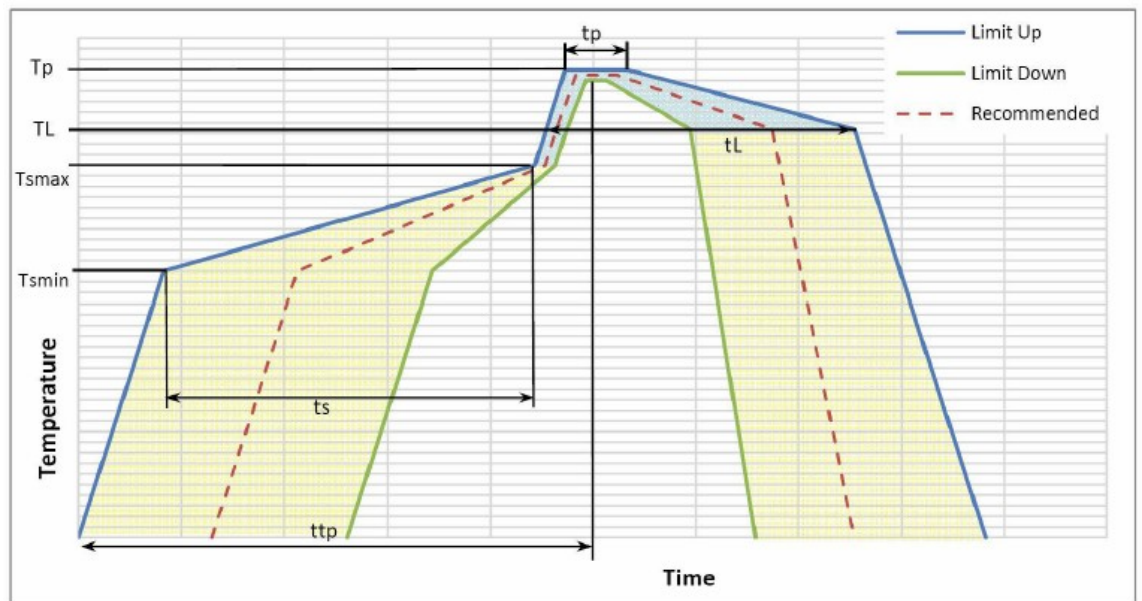
## 13.7. Solder Paste

Solder Paste	Lead free
	Sn/Ag/Cu

We recommend using only “no clean” solder paste in order to avoid the cleaning of the modules after assembly.

### 13.7.1. Solder Reflow

The following is the recommended solder reflow profile:



Profile Feature	Pb-Free Assembly
Average ramp-up rate ( $T_L$ to $T_P$ )	3°C/second max
Preheat	
- Temperature Min ( $T_{smin}$ )	150°C
- Temperature Max ( $T_{smax}$ )	200°C
- Time (min to max) ( $t_s$ )	60 ~ 180 seconds
$T_{smax}$ to $T_L$	
- Ramp-up Rate	3°C/second max
Time maintained above:	
- Temperature ( $T_L$ )	217°C
- Time ( $t_L$ )	60 ~ 150 seconds



Profile Feature	Pb-Free Assembly
Peak Temperature ( $T_P$ )	245 +0/-5°C
Time within 5°C of actual Peak Temperature ( $t_P$ )	10 ~30 seconds
Ramp-down Rate	6 °C/second max
Time 25°C to Peak Temperature	8 minutes max



**NOTE:**

All temperatures refer to topside of the package, measured on the package body surface.



**WARNING:**

The DE910 module withstands one reflow process only.



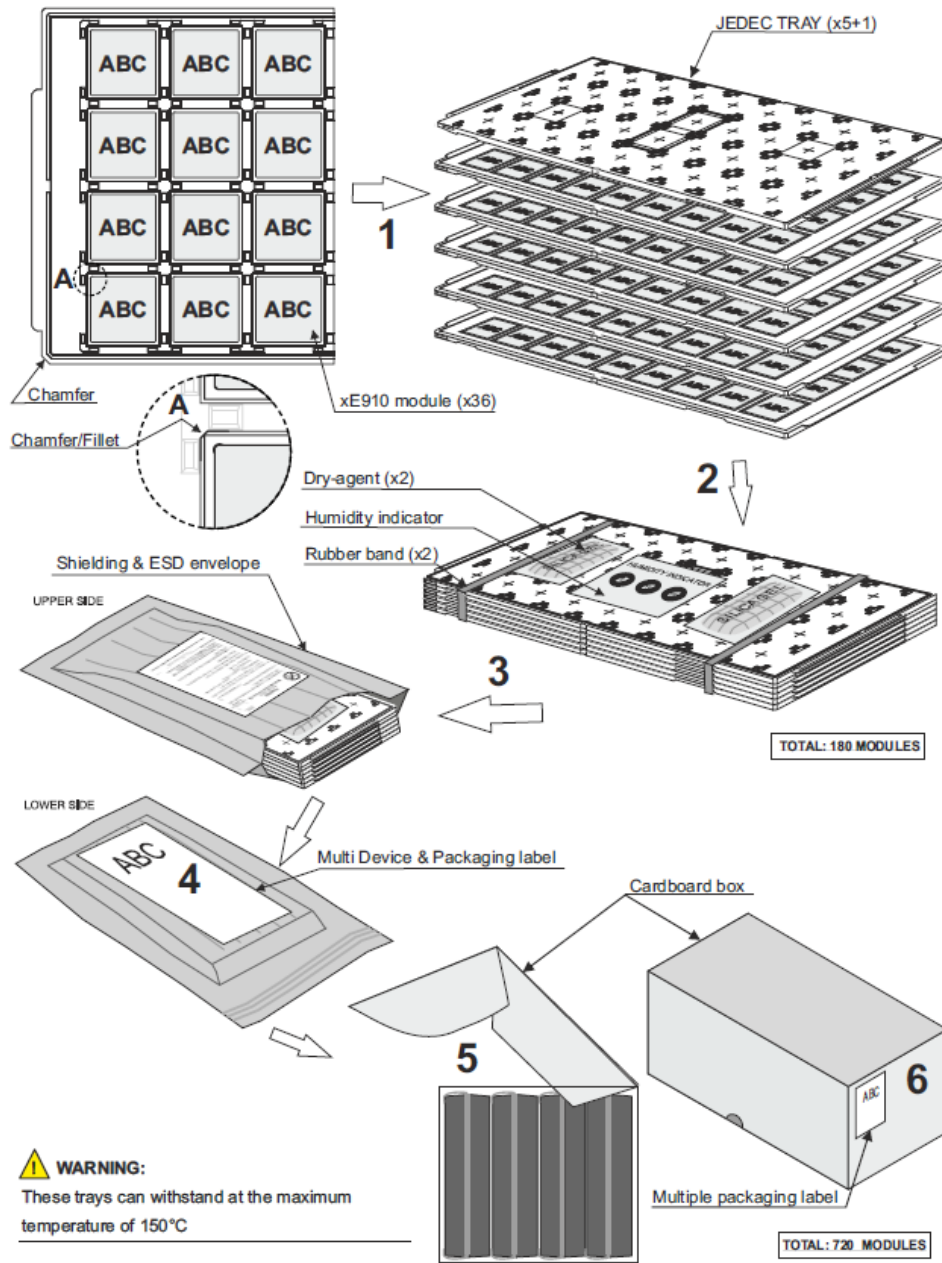
## 14. Packing System

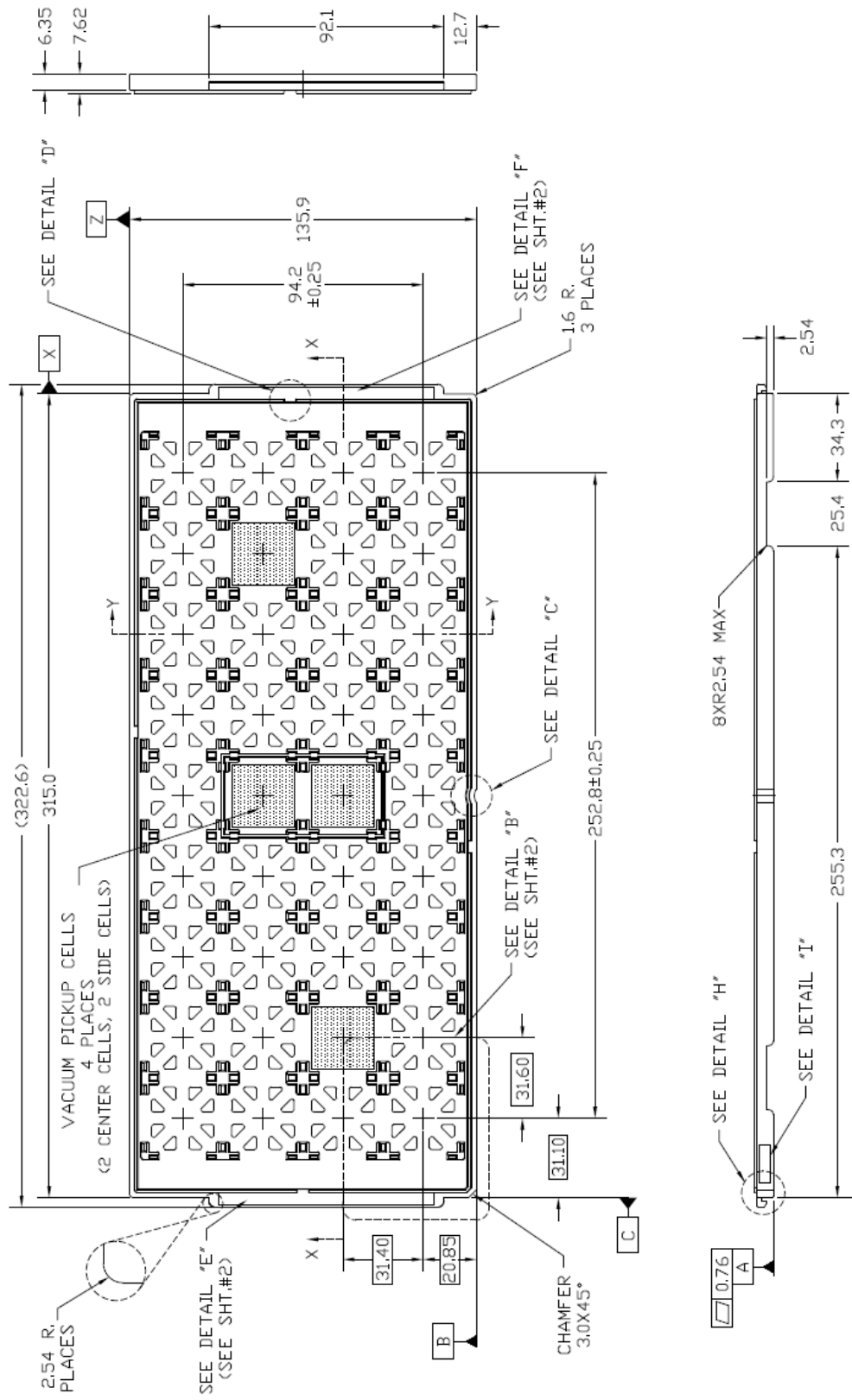
### 14.1. Tray

The DE910 modules are packaged on trays of 36 pieces each. These trays can be used in SMT processes for pick & place handling.



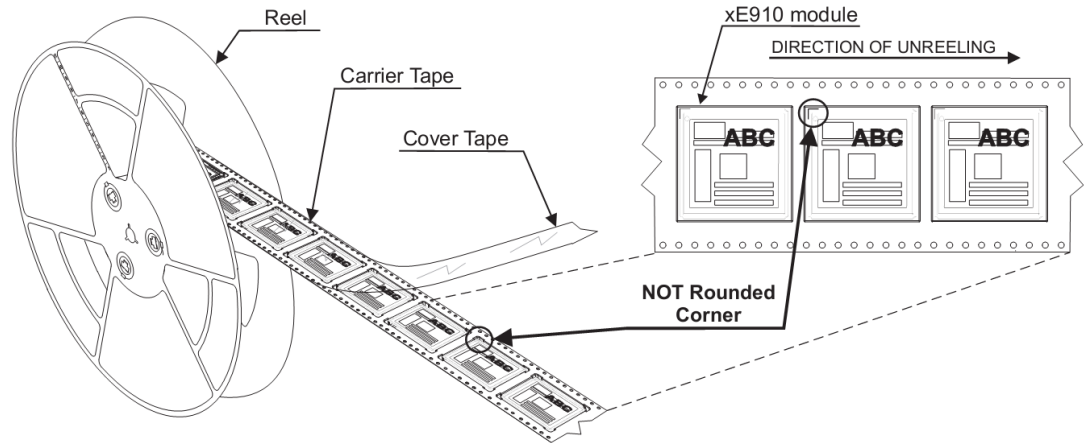




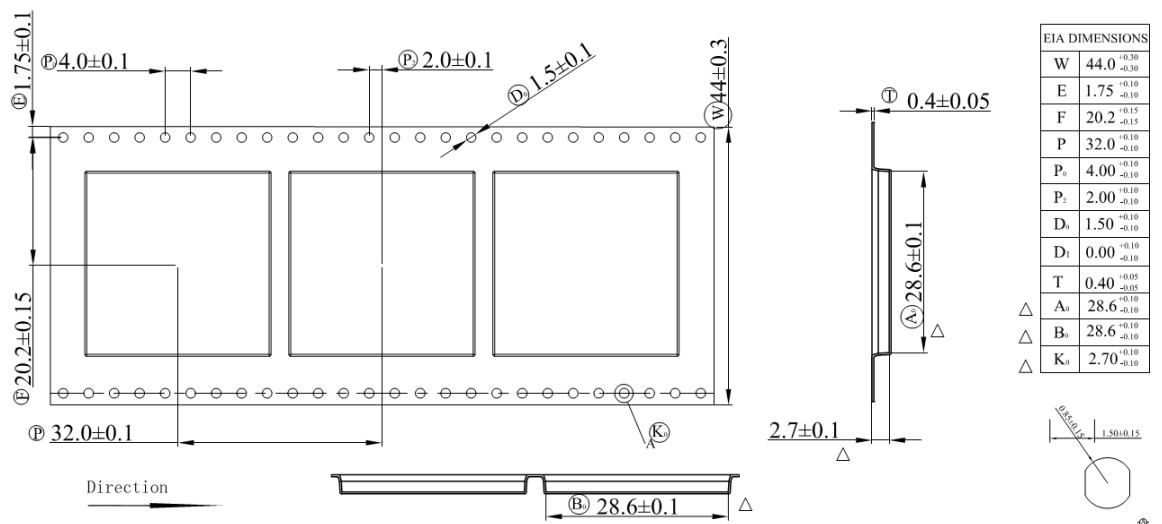


## 14.2. Reel

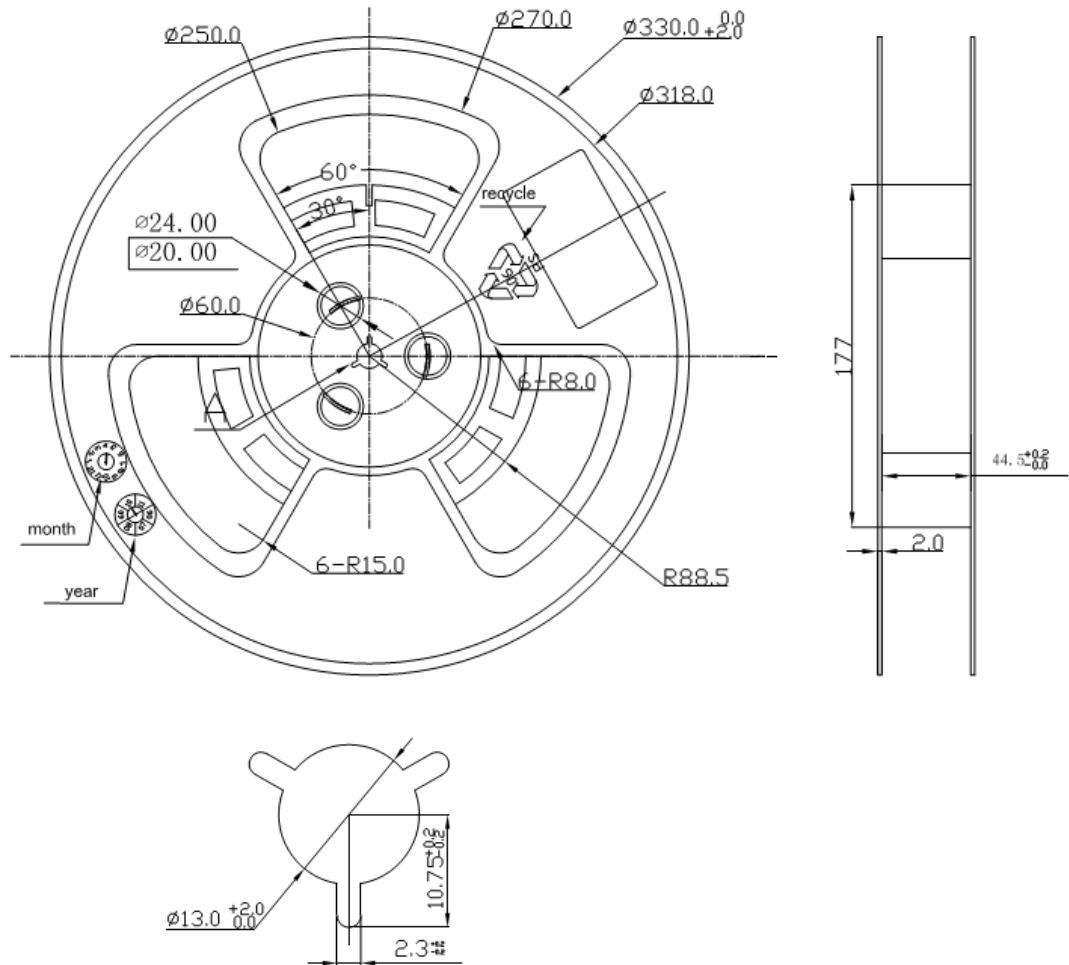
The DE910 can be packaged on reels of 200 pieces each.  
See figure for module positioning into the carrier.



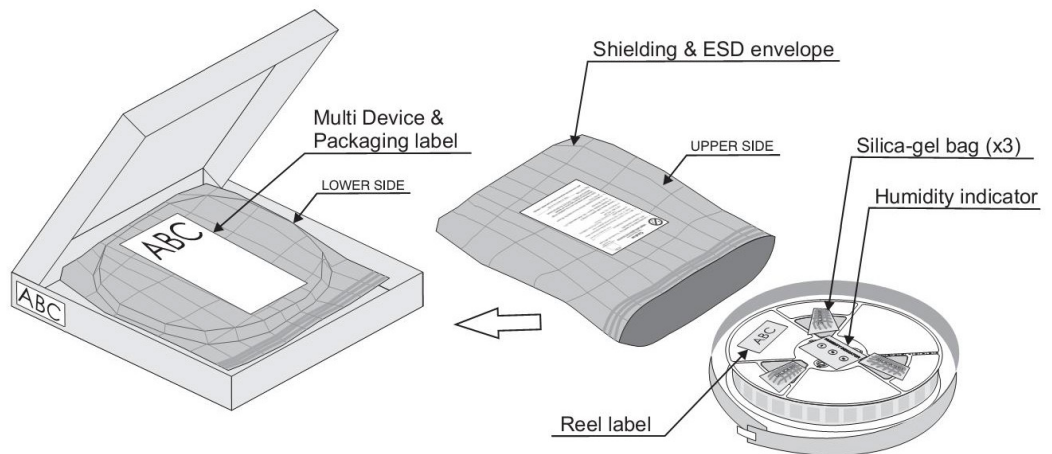
### 14.2.1. Carrier Tape Detail



### 14.2.2. Reel Detail



### 14.2.3. Packaging Detail





### 14.3. Moisture Sensibility

The DE910 is a Moisture Sensitive Device level 3, in accordance with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- a) Calculated shelf life in sealed bag: 12 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity (RH).
- b) Environmental condition during the production: - c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
- d) Baking is required if conditions b) or c) are not respected
- e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more





## 15. Application Design Guide

### 15.1. Download and Debug Port

One of the following options should be chosen in the design of host system in order to download or upgrade the Telit's software and debug DE910 when DE910 is already mounted on a host system.

#### **Users who use both of UART and USB interfaces to communicate DE910**

- Must implement a download method in a host system for upgrading DE910 when it's mounted.

#### **Users who use USB interface only to communicate DE910**

- Must arrange UART port in a host system for upgrading or debugging DE910 when it's mounted.

#### **Users who use UART interface only to communicate DE910**

- Must arrange USB port in a host system for upgrading or debugging DE910 when it's mounted.







The following regulatory and safety notices must be published in documentation supplied to the end user of the product or system incorporating an adapter in compliance with local regulations.

- Host system including DE910 must be labeled with  
“Contains transmitter module with  
FCC ID: RI7DE910-DUAL and IC ID: 5131A-DE910DUAL”

Les notices de normalisation et de sécurité doivent se trouver dans la documentation fournie à l'utilisateur du produit ou du système incorporant un adaptateur conforme aux réglementations locales.

- Le système hôte comprenant DE910 doit être marqué avec « Contient un module émetteur avec IDENTIFICATION FCC : RI7DE910-DUAL et identification IC : 5131A-DE910DUAL »







## 18. Document History

Revision	Date	Changes
0	2011-12-09	Release for Beta samples
1	2012-03-07	Release for Verizon
2	2012-07-03	Verizon TA update 8.2. Modem Serial Port2 12.2. Module Finishing & Dimensions
3	2012-12-20	3.1. Pin-out : Auxiliary UART and RUIIM IF 3.1.1. LGA Pads Layout 5.1. Power Supply Requirements 8.1. Modem Serial Port1 14.1 Download and Debug Port
4	2013-04-08	3. DE910 Module Connections 3.1. Pin-Out 5.1. Power Supply Requirements 8.1. Modem Serial Port1
5	2013-04-16	12.4. Stencil
6	2013-06-03	2.2. Product Specifications
7	2013-11-26	2.2. Product Specifications 4.2. Turning off the DE910 module 5.2.6. Power Supply PCB layout Guidelines 6.3.3. The Design Considerations to enhanced GNSS performance 12.7.1. Solder Reflow 13. Packing System
8	2014-11-12	3. DE910 module connections 6.1.2. PCB Guidelines in case of FCC certification 10.6. RTC Bypass Output
9	2016-09-14	14.1 New tray information

