GL865/GL868 V3, GE866 Digital Voice Interface

Application Note

80000NT10104A Rev. 2 – 2014-04-16

APPLICABILITY TABLE

	SW Versions
GL Family (Embedded)	
GL865-DUAL V3	16.00.xx2
GL865-QUAD V3	
GL868-DUAL V3	
GE866-QUAD	16.00.xx3

Note: the features described in the present document are provided by the products equipped with the software versions equal or higher than the versions shown in the table. See also the Document History chapter.

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Contents

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Tables

1. Introduction

The present document provides the reader with a guideline concerning the setting and use of the Digital Voice Interface developed on the Telit's modules shown in the Applicability Table.

1.1. Scope

This Application Note covers the configurations of the Digital Voice Interface, e.g.: the selections of the voice sampling frequency, the bit number of the voice sample, the audio formats, etc. In addition, the document shows some configurations of a popular Audio Codec connected to the module. These activities are accomplished via I^2S and I^2C buses; the hardware characteristics of the two buses are beyond the scope of the document.

1.2. Audience

The document is intended for those users that need to develop applications dealing with signal voice in digital format.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

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Telit appreciates feedback from the users of our information.

1.4. Related Documents

[1] GL865-DUAL/QUAD V3 Hardware User Guide, 1vv0301018
[2] MAX9867 Ultra-Low Power Stereo Audio Codec, MAXIM
[3] AT Commands Reference Guide, 80000ST10025A
[4] GL868-DUAL V3 Hardware User Guide, 1vv0301061
[5] GE866-DUAL Hardware User Guide, 1vv0301051

1.5. Document History

Revision	Date	Products / SW Versions	Changes
0	2013-09-09	/	First issue
1	2014-03-06	/	Chapter 4: Added the sentence: "The Digital Voice Interface supports the Echo canceller functionality, refer to document [3] for the specific AT commands"
2	2014-04-16	/	The document title has been changed from "GL865/GL868 V3 Digital Voice Interface" into "GL865/GL868 V3, GE866 Digital Voice Interface". The note about the Echo canceller has been moved into chapter 2 The chapters numbering/naming has been reorganized.
		Products added: GE866-QUAD/16.00.xx3	/

1.6. Abbreviations and Acronyms

DTE Data Terminal Equipment
DVI Digital Voice Interface
GPIO General Purpose Input/Output
I2C Inter-Integrated Circuit
I2S Inter-IC Sound
MSB Most Significant Bit

2. DVI Overview

Before dealing with the configuration and technical aspects of the Telit's Digital Voice Interface (DVI) it is useful to illustrate briefly how this interface can be used, refer to fig. 1.

The voice coming from the downlink, in digital format, is captured by the dedicated software running on the Telit's module and directed to the Digital Voice Interface. The Audio Codec decodes the voice and sends it to the speaker. The voice captured by the microphone is coded by the Audio Codec and directed through the Digital Voice Interface to the module that collects the received voice, in digital format, and sends it on the uplink.

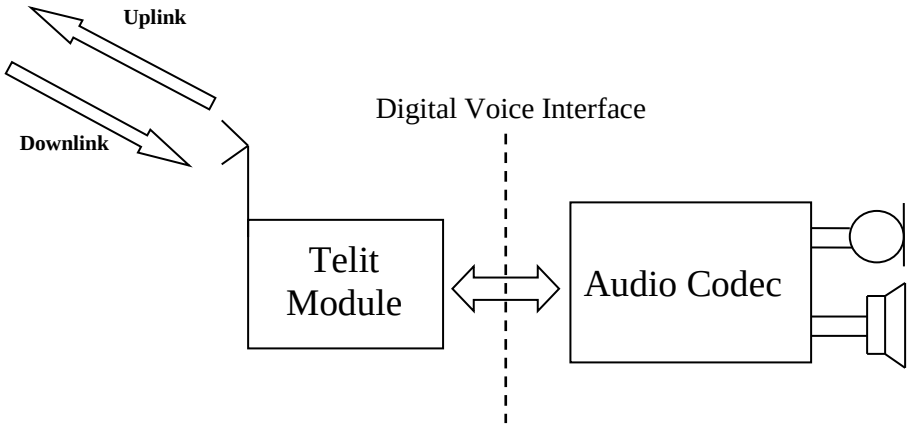


fig. 1: Example of Digital Voice Interface Use

NOTICE: the Digital Voice Interface supports the Echo canceller functionality, which is beyond the scope of the present document. Refer to document [3] for the specific AT commands.

3. DVI Bus

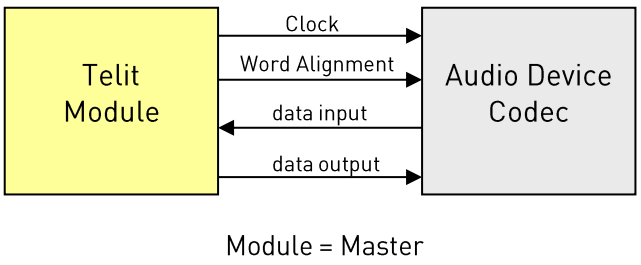
The physical DVI interface provided by the modules of the Telit's GL family is based on the standard I^2S Bus. An overview of the standard I^2S Bus is described in chapter 6.1. Tab. 1 summarizes the DVI signals and a short description for each one of them; refer to documents [1], [4], or [5] to have information on electrical characteristics and signals pin-out.

DVI Signal	DVI Signal name	Description
Clock	DVI_CLK	Data Clock
Word Alignment	DVI_WAO	Frame Synchronism
serial audio data input	DVI_RX	Received Data
serial audio data output	DVI_TX	Transmitted Data

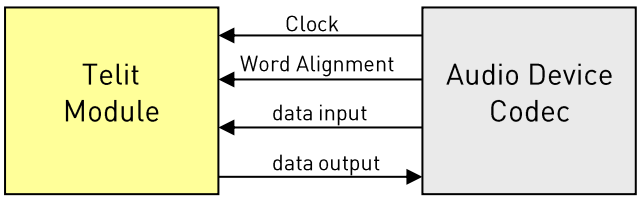
Tab. 1: DVI Signals

The figures below show the two configurations of the DVI interface relating to the Word Alignment and Clock signals. When the module is Master the Clock and Word Alignment signals (also called Word Alignment Output WAO) are generated by the module itself, otherwise, when it is Slave, both signals are generated by the connected Audio Device Codec.

In general, before establishing a voice call it is possible to select one of the two configurations and in accordance with the selected setting, configure the module and the codec via the AT commands provided by Telit [3]. The next pages describe the use of these AT commands.



Module = Master



Module = Slave

fig. 2: Master and Slave Configurations

4. DVI AT Commands

Several DVI audio bus configurations are available via AT#DVI and AT#DVIEXT commands. The tables in the following sub-sections summarize their parameters; refer to document [3] for AT commands syntax details.

4.1. AT#DVI

AT#DVI command enables/disables the DVI interface, selects the DVI port, and sets the module in Master or Slave configuration.

The following table shows the AT command parameters values.

AT#DVI =<mode>,<dviport>,<clockmode>		
<mode>	<dviport>	<clockmode>
0 →disable DVI interface 1 → enable DVI interface 2 → reserved	1 → select DVI port 1, factory setting 2 → reserved	0 → DVI slave 1 → DVI master, factory setting

Tab. 2: DVI configuration via AT#DVI command

4.2. AT#DVIEXT

AT#DVIEXT command sets the module in Normal or Burst DVI Audio Format:

- In Normal DVI Audio Format the WAO signal defines the left and right audio channel.
- In Burst DVI Audio Format the WAO signal defines the beginning of the audio frame.

The following table shows the AT command parameters values.

DVI Audio Format (Mode)	AT#DVIEXT <config>,<samplerate>,<samplewidth>,<audiomode>,<edge>				
	<config>	<samplerate>	<samplewidth>	<audiomode>	<edge>
Normal (I^2S)	1	0 → 8 [KHz] sample rate 1 → reserved	0 → 16 bits per sample 1 → reserved 2 → reserved 3 → 24 bits per sample 4 → 32 bits per sample	0 → Mono 1 → Dual Mono The same Data Word is transmit ted on both audio channels (right and left) 2 → reserved	0 → data is transmitted on the falling edge of the clock and sampled on its rising edge, factory setting. 1 → data is transmitted on the rising edge of clock and sampled on its falling edge.
Burst (PCM)	0 factory setting				1 → the rising edge of the clock is used to shift out the next data to transmit. The received data bit is captured on the falling edge of the clock. 0 → has the same behavior of 1.

Tab. 3: DVI Audio Format configuration via AT#DVIEXT command

5. DVI Setting Examples

The next chapters show examples concerning the audio formats supported by the DVI audio bus in Master and Slave configurations. All the following setting examples are performed using the hardware configuration shown in fig. 3. I²C bus is used to configure the MAX9867 Codec[1] [2]: the user by means of AT commands can control the codec. The DVI bus provides the voice connection between the two devices.

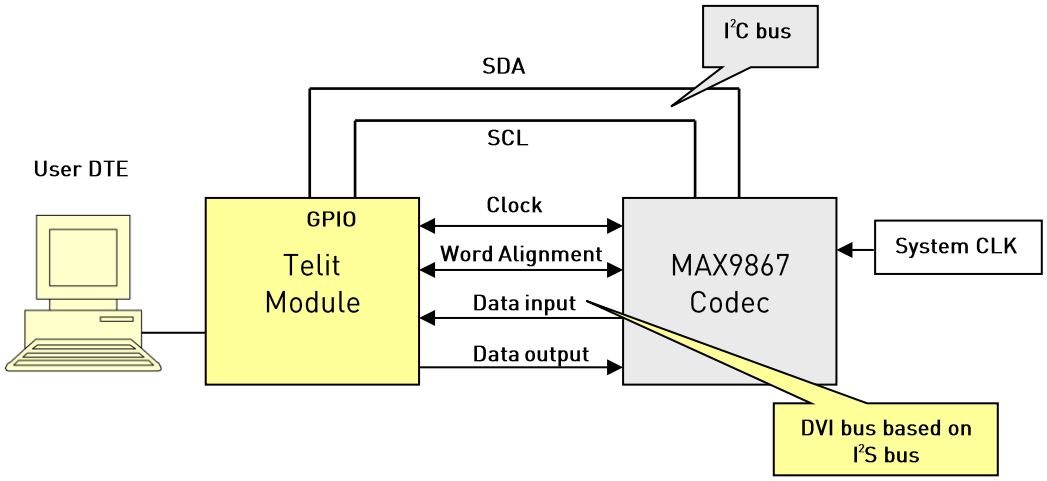


fig. 3: Telit Module/Codec Connections

The setting examples are organized as shown in the figure below.

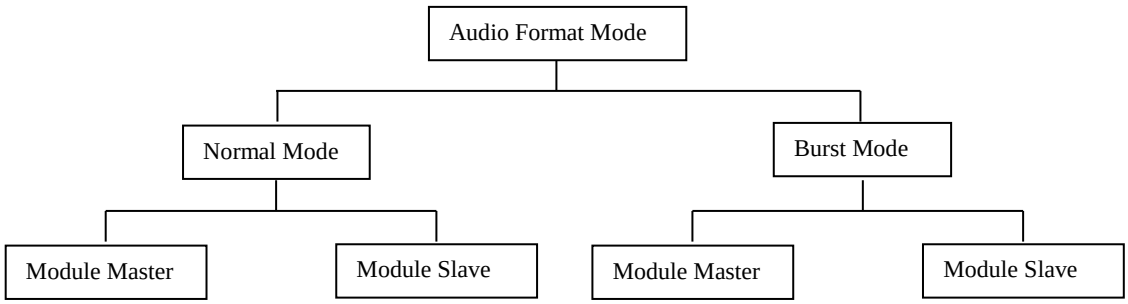


fig. 4: DVI Configurations

[1] The following examples use the MAX9867 Codec, see chapter 6.2 for a schematic reference design. In general, the user can use any codec compliant with the technical requirements of the used module.

5.1. Normal (I^2S) Mode

5.1.1. Module is Master

The fig. 5 shows a timing diagram that refers to the module in the role of master. In this case, the WAO and CLK signals are generated by the module. The WAO signal defines the frame of the two audio channels: left and right.

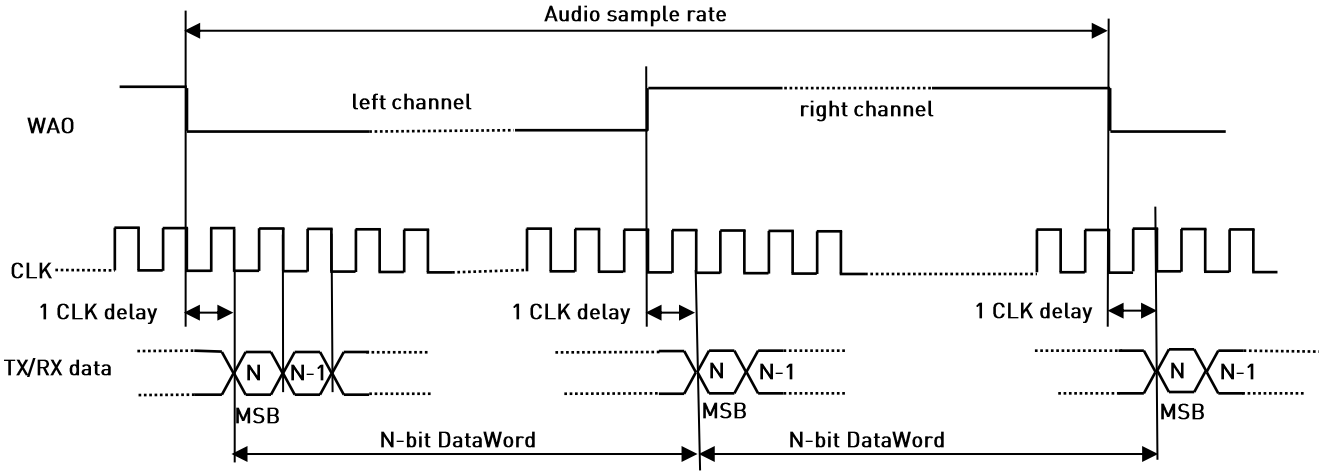


fig. 5: Module is Master/Normal mode/ N bits per sample/Dual Mono

When module is Master the BitClockFrequency (CLK) is provided by the following expression:

$$BitClockFrequency = DataWordBit \times ChannelNumber \times AudioSampleRate$$

Refer to Tab. 4 for the BitClockFrequency generated by the module.

<samplewidth>	DataWordBit	Audio channels	AudioSampleRate: 8 KHz
			BitClockFrequency in KHz
0	16	2	256
1	reserved		
2	reserved		
3	24	2	384
4	32	2	512

Tab. 4: BitClockFrequency generated by the module in Master/Normal Mode

Here are the lists of AT commands used to set the module in Master Normal (I^2S) Mode, and configure the codec in accordance with the module setting. After each command is described the used parameters values meaning.

Configure the module in Master Normal (I^2S) Mode

DVI bus

AT#DVI=1,1,1
OK

1 enable DVI interface
1 use DVI port 1 (mandatory)
1 set the module as Master (factory setting)

AT#DVIEXT=1,0,0,1,0
OK

1 Normal Mode
0 sample rate 8 KHz (mandatory)
0 16 bits per sample
1 Dual Mono, the same Data Word is transmitted on both audio channels
0 data is transmitted on falling edge of clock and sampled on rising edge of clock

Configure the codec in Slave Normal (I^2S) Mode

I^2C bus

AT#I2CWR=X,Y,30,4,19
>00109000100A330000330C0C09092424400060
OK

X GPIO number used as SDA, refer to [3]
Y GPIO number used as SCL, refer to [3]
30 Device address on I^2C, refer to [2]
4 Register address from which start the writing, refer to [2]
19 number of bytes to write
>00109000…..refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA, refer to [3]
Y GPIO number used as SCL, refer to [3]
30 Device address on I^2C, refer to [2]
17 Register address where write data, refer to [2]
1 number of bytes to write
>8A refer to [2]

The fig. 6 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (256 KHz) and WAO signals are generated by the module.

Left channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

Right channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

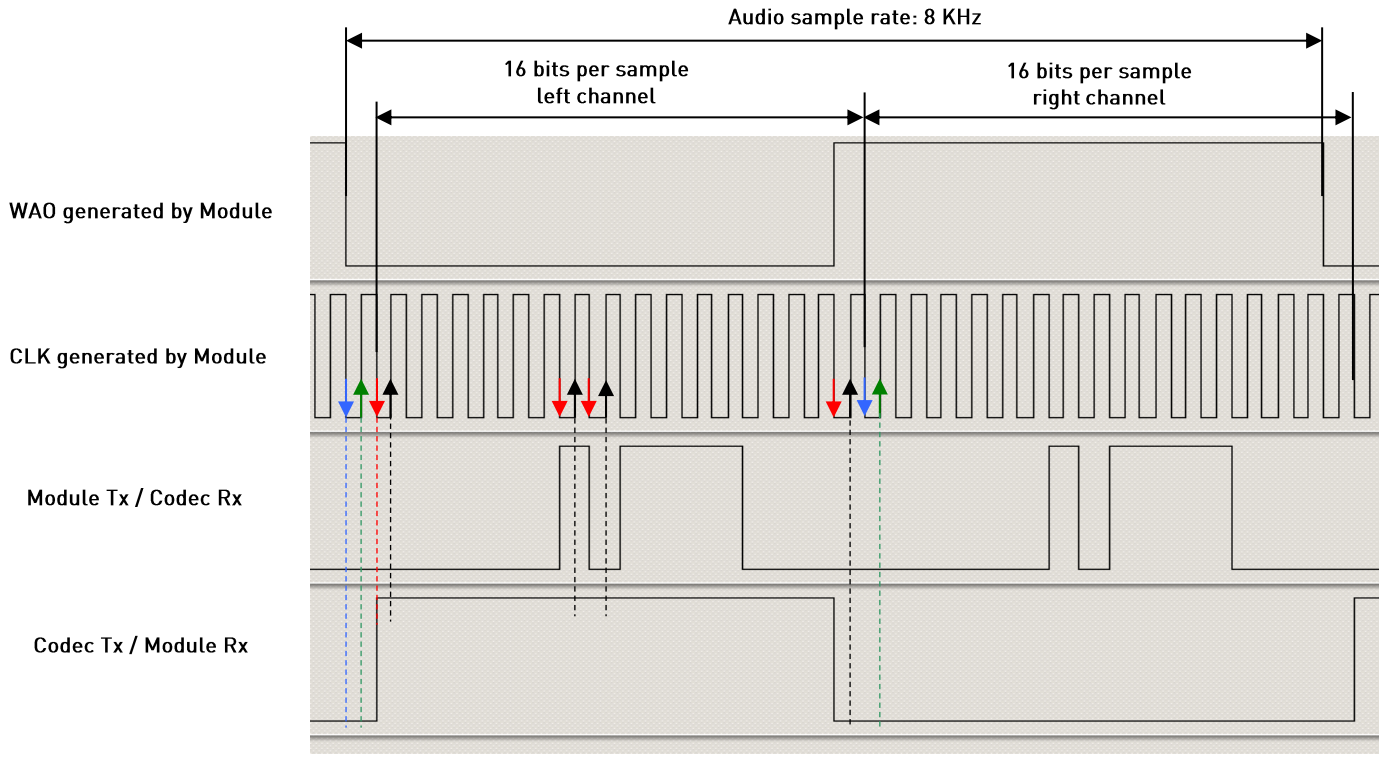


fig. 6: Module is Master/Normal mode/16 bits per sample/Dual Mono/<edge>=0

5.1.2. Module is Slave

Here are the lists of the AT commands used to set the module in Slave Normal (I^2S) Mode, and configure the Codec in accordance with the module setting. After each command is described the used parameters values meaning.

Configure the Module in Slave-Normal (I^2S) Mode

DVI bus

AT#DVI=1,1,0
OK

1	enable DVI interface
1	use DVI port 1 (mandatory)
0	set the module as Slave

AT#DVIEXT=1,0,3,1,0
OK

1	Normal Mode
0	sample rate 8 KHz (mandatory)
3	24 bits per sample
1	Dual Mono, the same Data Word is transmitted on both audio channels
0	data is transmitted on falling edge of clock and sampled on rising edge of clock

Configure the Codec in Master-Normal (I^2S) Mode

I^2C bus

AT#I2CWR=X,Y,30,4,19
>0010100090023300003 30C0C09092424400060
OK

X	GPIO number used as SDA
Y	GPIO number used as SCL
30	Device address on I2C
4	Register address from which start the writing
19	number of bytes to write
>00101000…..refer to [2]	

AT#I2CWR=X,Y,30,17,1
>8A
OK

X	GPIO number used as SDA
Y	GPIO number used as SCL
30	Device address on I2C
17	Register address where write data
1	number of bytes to write
>8A	refer to [2]

NOTICE: *the Codec is in Master configuration and generates a clock equal to 384 KHz. On the module the selected number of bits per sample is 24, see Tab. 4*

The fig. 7 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (384 KHz) and WAO signals are generated by the codec.

Left channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

Right channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

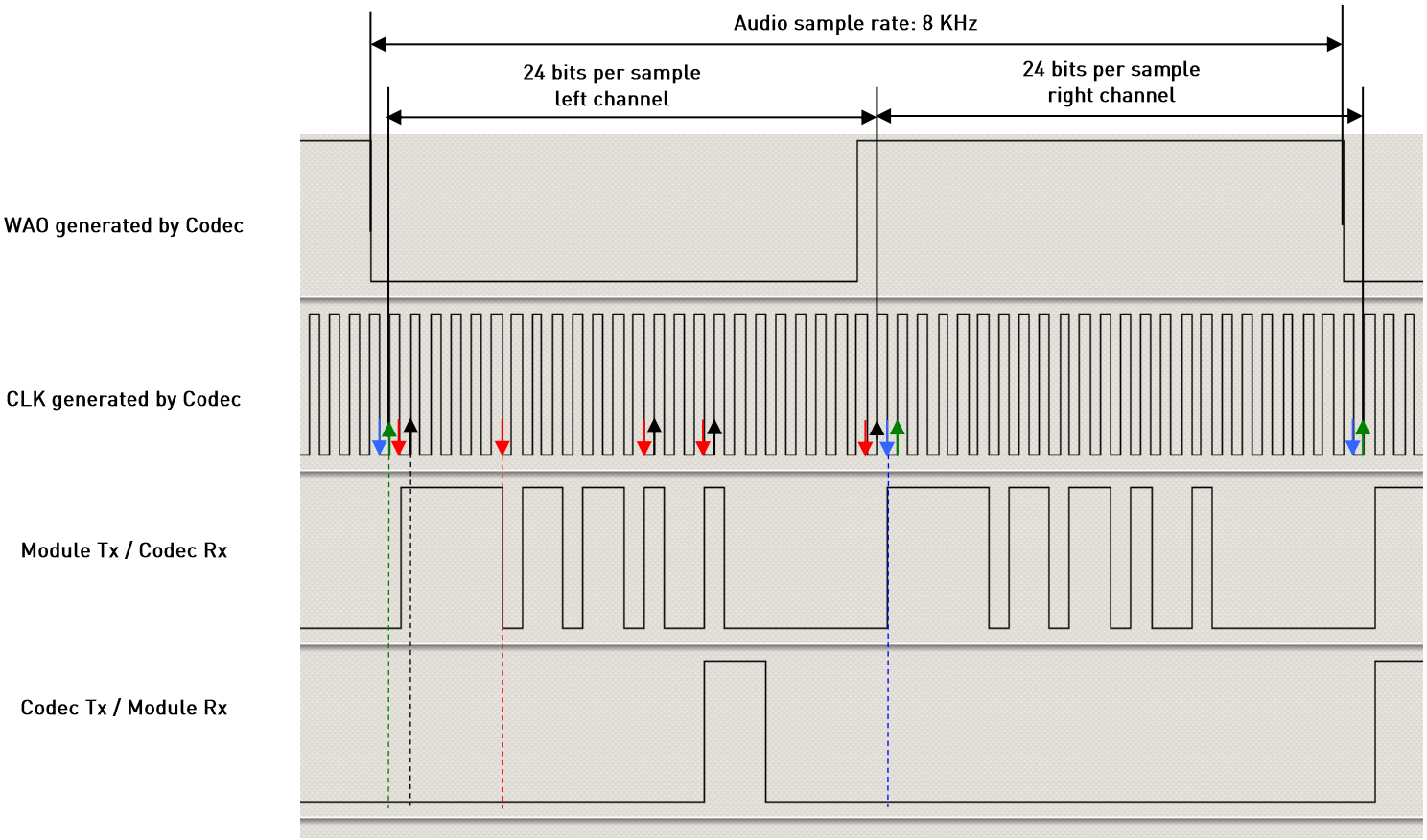


fig. 7: Module is Slave/Normal mode/24 bits per sample/Dual Mono/<edge>=0

5.2. Burst Mode (PCM)

5.2.1. Module is Master

The fig. 8 shows a timing diagram that refers to the module in the role of master. In this case, the WAO and CLK signals are generated by the module. The WAO signal defines the frame of the audio channel.

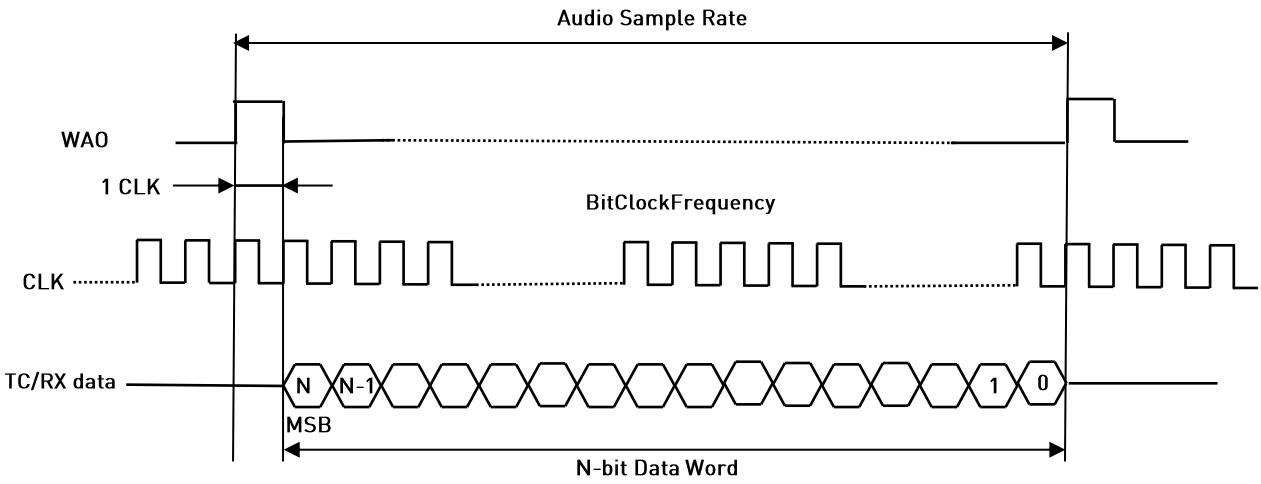


fig. 8: Module is Master/Burst mode/N bits per sample/Mono Mode

When module is Master the BitClockFrequency (CLK) is provided by the following expression:

$$BitClockFrequency = (DataWordBit + 1) \times AudioSampleRate$$

Refer to Tab. 5 for the BitClockFrequency generated by the Module.

<samplewidth>	DataWordBit	Audio channels	AudioSampleRate: 8 KHz
			BitClockFrequency in KHz
0	16 (+ 1[2])	1	136
1	reserved		
2	reserved		
3	reserved		
4	32 (+ 1)	1	264

Tab. 5: BitClockFrequency generated by the module in Master/Burst Mode

[2] The width of the WAO pulse is 1 CLK.

Below is the list of the AT commands used to set the module in Master Burst (PCM) Mode, and configure the codec in accordance with the current module setting.

Configure the module in Master-Burst (PCM) Mode

DVI bus

AT#DVI=1,1,1
OK

1 enable DVI interface
1 use DVI port 1 (mandatory)
1 set the module DVI as Master (factory setting)

AT#DVIEXT=0,0,0,0,1
OK

0 Burst Mode (PCM) (factory setting)
0 sample rate 8 KHz (mandatory)
0 16 bits per sample
0 Mono Mode
1 the rising edge of the clock is used to shift out the next data to transmit. The received data bit is captured on the falling edge of the clock (0 has the same behavior).

Configure the codec in Slave Burst (PCM) Mode.

I^2C bus

AT#I2CWR=X,Y,30,4,19
> 00109000600A330000330C0C09092424400060

OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
4 Register address from which start the writing
19 number of bytes to write
>00109000…..refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
17 Register address where write data
1 number of bytes to write
>8A refer to [2]

The fig. 9 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (136 KHz) and WAO signals are generated by the module.

↑: Data transitions occur on the rising edge of the CLK

↓: Data are latched on the falling edge of the CLK

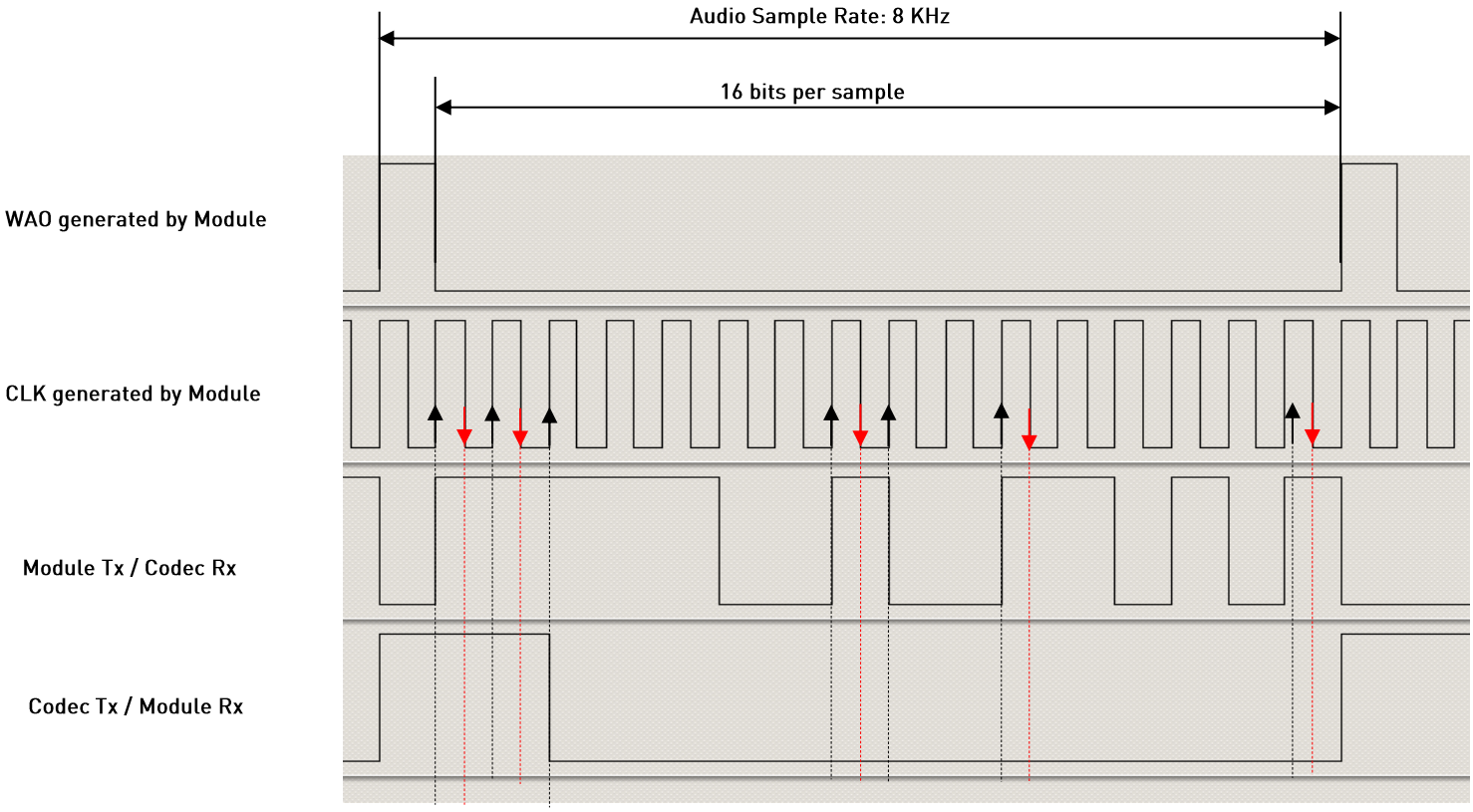


fig. 9: Module is Master/Burst Mode/16 bits per Sample/Mono Mode/<edge>=1

5.2.2. Module is Slave

The fig. 10 shows a timing diagram that refers to the codec in master configuration. In this case, the WAO and CLK signals are generated by the codec.

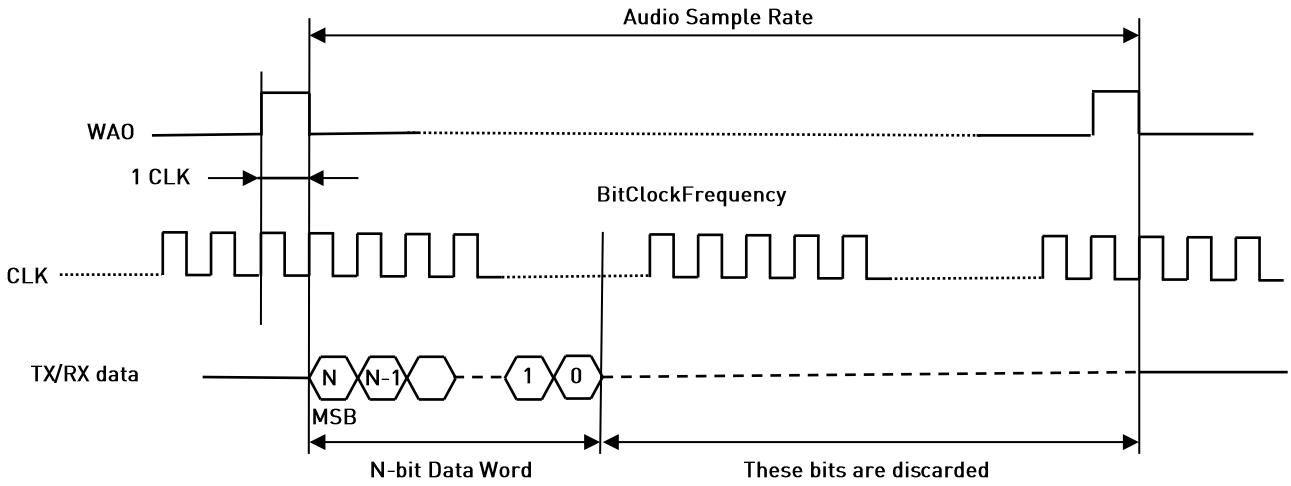


fig. 10: Module is Slave/Burst mode/N bits per sample/Mono Mode

Here are the lists of AT commands used to set the module in Slave Burst (PCM) Mode, and configure the Codec in accordance with the current module setting. After each command is described the used parameters values meaning.

Configure the module in Slave Burst (PCM) Mode.

DVI bus

AT#DVI=1,1,0
OK

1 enable DVI interface
1 use DVI port 1 (mandatory)
0 set the module as Slave

AT#DVIEXT=0,0,0,0,1
OK

0 Burst Mode (factory setting)
0 sample rate 8 KHz (mandatory)
0 16 bits per sample
0 Mono Mode
1 the rising edge of the clock is used to shift out the next data to transmit. The received data bit is captured on the falling edge of the clock (0 has the same behavior).

Configure the Codec in Master Burst PCM Mode.

I^2C bus

AT#I2CWR=X,Y,30,4,19
> 00101000A40A330000330C0C09092424400060
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
4 Register address from which start the writing
19 number of bytes to write
>00101000…..refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
17 Register address where write data
1 number of bytes to write
>8A refer to [2]

The fig. 11 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (384 KHz) and WAO signals are generated by the codec.

↑: Data transitions occur on the rising edge of the CLK

↓: Data are latched on the falling edge of the CLK

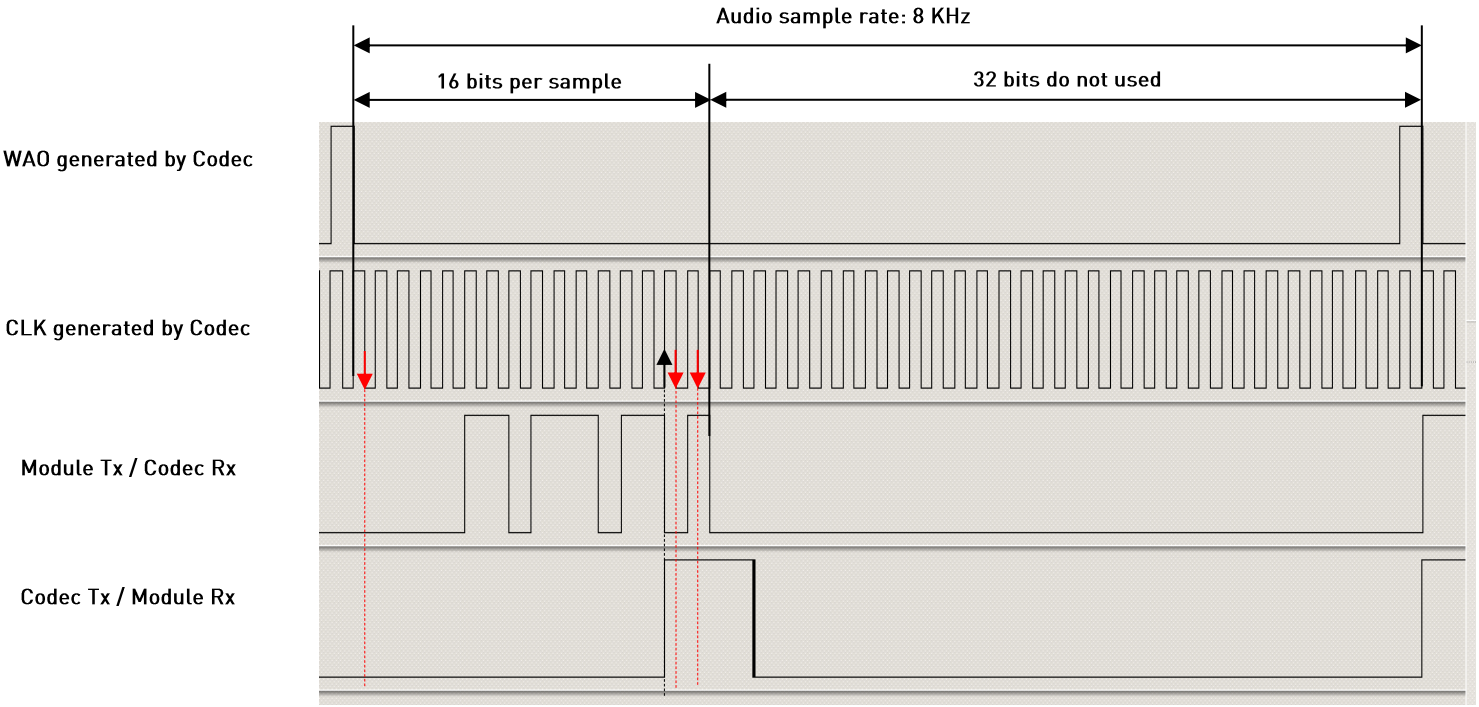


fig. 11: Module is Slave/Burst mode/16 bits per sample/Mono Mode/<edge>=1

6. Annex

6.1. I²S Bus Overview

This chapter provides a short description of the standard I²S bus. This standard suitably modified is used by the DVI interface implemented on the Telit modules.

The standard I²S is an electrical serial bus designed for connecting digital audio devices. This popular serial bus has been developed by Philips® in 1986 as a 3-wire bus for interfacing to audio chips such as codecs. It is a simple data interface, without any form of address or device selection.

Refer to fig. 12: the I²S design handles audio data separately from clock signals. On an I²S bus, there is only one bus master and one transmitter.

In high-quality audio applications involving a codec, the codec is typically the master so that it has precise control over the I²S bus clock.

An I²S bus design consists of the following serial bus lines:

- SD: Serial Data
- WS: Word Select
- Serial Clock: SCK

The I²S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.

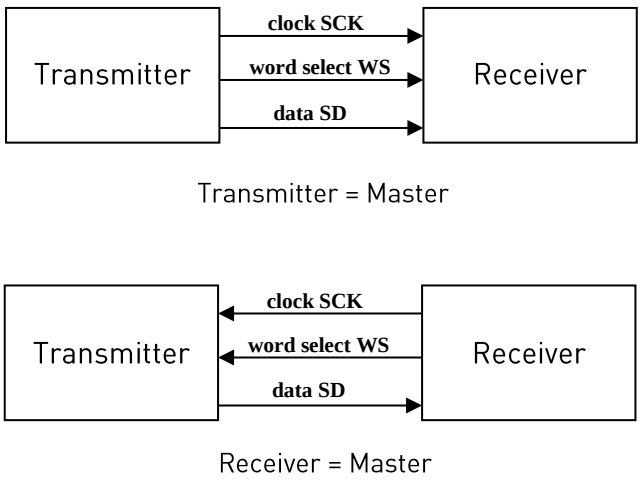


fig. 12: I2S Bus Configurations

6.2. Schematic

A schematic example of an interface between a Telit Module and the MAX9867 Codec could be the following:

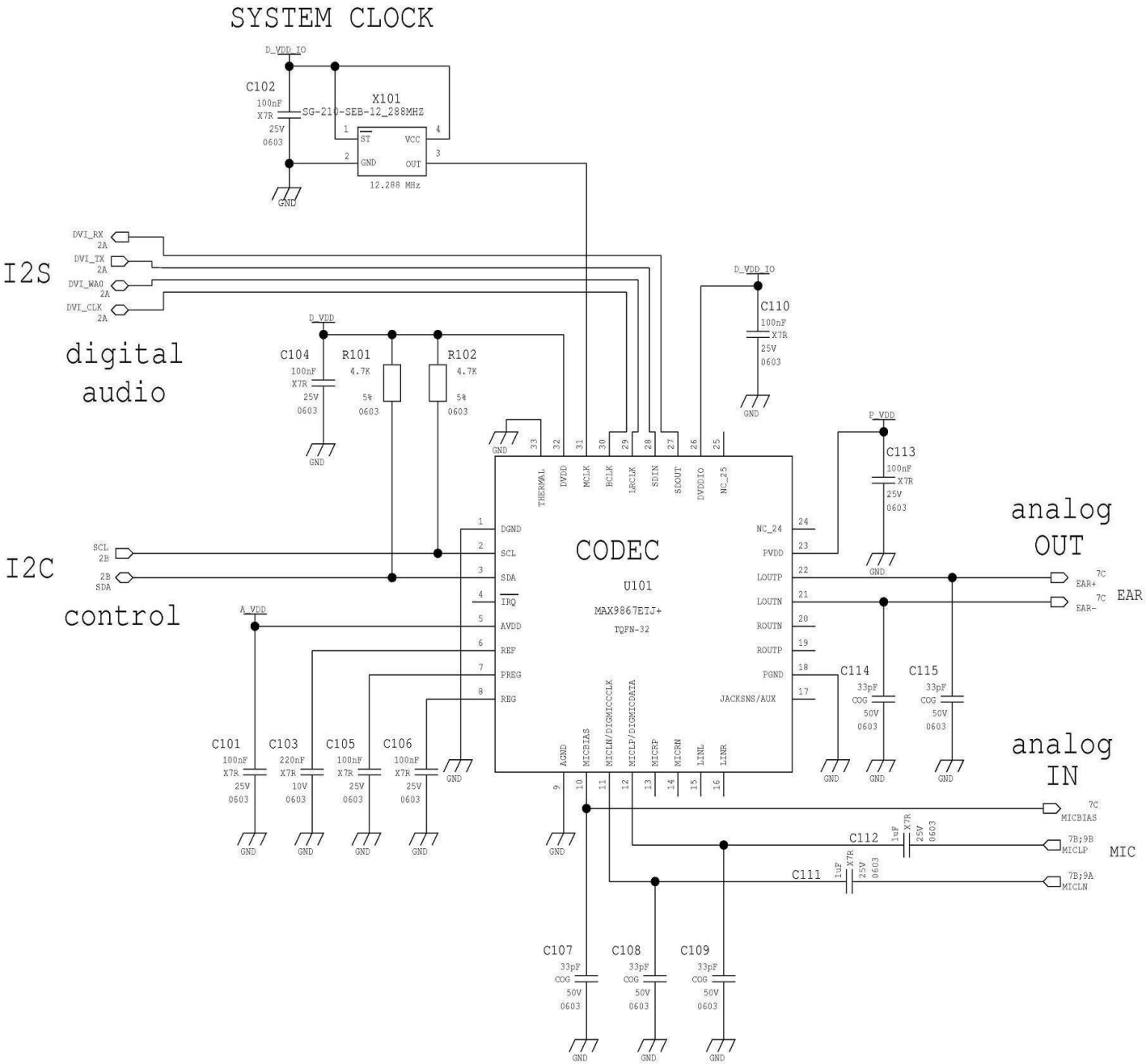


fig. 13: Schematic for Reference Design