HE/UE910, UL865 Digital Voice Interface Application Note

80000NT10050A Rev. 6 – 2014-04-16

APPLICABILITY TABLE

	SW Versions
HE910 Family	
HE910 [1]	12.00.xx3
HE910-GA	12.00.xx3
HE910-EUR	12.00.xx3
HE910-NAR	12.00.xx3
UE/UL Family (Embedded)	
UE910-EUR	12.00.xx4
UE910-NAR	12.00.xx4
UL865-EUR	12.00.xx4
UL865-NAR	12.00.xx4
UL865-N3G	12.00.xx4

Note: the features described in the present document are provided by the products equipped with the software versions equal or higher than the versions shown in the table. See also the Document History chapter.

[1] HE910 is the "type name" of the products marketed as HE910-G & HE910-DG

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Contents

Figures

Tables

1. Introduction

The present document provides the reader with a guideline concerning the setting and use of the Digital Voice Interface developed on the Telit's modules families shown in the Applicability Table.

1.1. Scope

This Application Note covers the configurations of the Digital Voice Interface, e.g.: the selections of the voice sampling frequency, the bit number of the voice sample, the audio formats, etc. In addition, the document shows some configurations of a popular Audio Codec connected to the Module. These activities are accomplished via I^2S and I^2C buses; the hardware characteristics of the two buses are beyond the scope of the document.

1.2. Audience

The document is intended for those users that need to develop applications dealing with signal voice in digital format.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

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Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.
Telit appreciates feedback from the users of our information.

1.4. Related Documents

[1] HE910 Hardware User Guide, 1vv0300925
[2] MAX9867 Ultra-Low Power Stereo Audio Codec, MAXIM
[3] HE910/UE910/UL865 AT Commands Reference Guide, 80378ST10091A
[4] UE910 Hardware User Guide, 1vv0301012
[5] UL865 Hardware User Guide, 1vv0301050

1.5. Document History

Revision	Date	Products/SW Versions	Changes
0	2011-07-11	/	First issue
1	2012-02-16	/	The present revision supersedes Rev. 0
2	2013-05-31	/	Updated all the screenshots of the timing diagrams. Added the AT commands list to set the codec in Slave-Burst (PCM) Mode configuration.
3	2013-06-20	/	The previous document title “HE910 Family Digital Voice Interface” has been changed in HE/UE910 Digital Voice Interface. In accordance with the new title, the Applicability Table has been updated.
4	2013-09-30	/	The previous document title “HE/UE910 Digital Voice Interface” has been changed in “HE/UE910, UL865 Digital Voice Interface”.
		Products added: UL865-EUR / 12.00.xx4 UL865-NAR / 12.00.xx4	/
5	2014-03-17	/	In the Applicability Table have been corrected the wrong products, turning them into UL865-EUR / 12.00.xx4 and UL865-NAR / 12.00.xx4
		Products added: UL865-N3G / 12.00.xx4	/
6	2014-04-16	/	The note about the Echo canceller has been added in chapter 2. The chapters numbering/naming has been reorganized.

1.6. Abbreviations and Acronyms

DTE	Data Terminal Equipment
DVI	Digital Voice Interface
GPIO	General Purpose Input/Output
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
MSB	Most Significant Bit

2. DVI Overview

Before dealing with the configuration and technical aspects of the Telit' Digital Voice Interface (DVI) it is useful to illustrate briefly where and how this interface can be used, refer to fig. 1

The voice coming from the downlink, in digital format, is captured by the dedicated software running on the Telit's module and directed to the Digital Voice Interface. The Audio Codec decodes the voice and sends it to the speaker. The voice captured by the microphone is coded by the Audio Codec and directed through the Digital Voice Interface to the module that collects the received voice, in digital format, and sends it on the uplink.

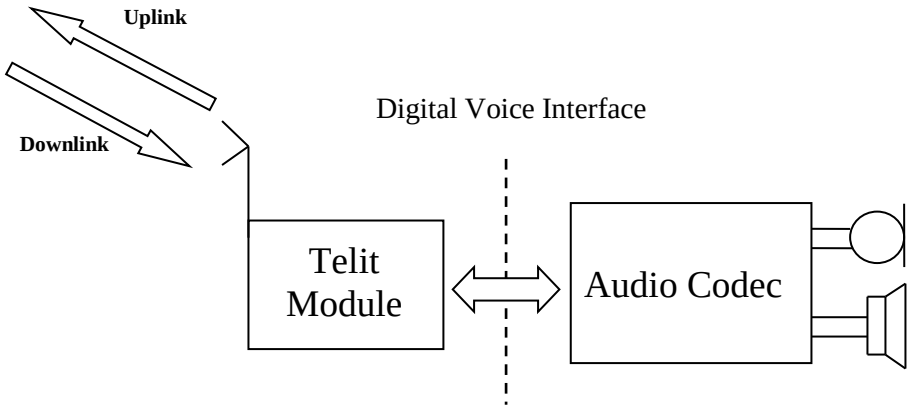

fig. 1: Example of Digital Voice Interface Use

NOTICE: the Digital Voice Interface supports the Echo canceller functionality, which is beyond the scope of the present document. Refer to document [3] for the specific AT commands.

3. DVI Bus

The physical DVI interface provided by the Telit's modules is based on the I^2S Bus. An overview of the standard I^2S Bus is described in chapter 6.1. Tab. 1 summarizes the DVI signals and a short description for each one of them: refer to documents [1], [4], and [5] to have information on electrical characteristics and signals pin-out in accordance with the used module.

DVI Signal	DVI Signal name	Description
Clock	DVI_CLK	Data Clock
Word Alignment	DVI_WAO	Frame Synchronism
serial audio data input	DVI_RX	Received Data
serial audio data output	DVI_TX	Transmitted Data

Tab. 1: DVI Signals

The figures below show the two configurations of the DVI interface relating to the Word Alignment and Clock signals. When the module is Master the Clock and Word Alignment signals (also called Word Alignment Output WAO) are generated by the module itself, otherwise, when it is Slave, both signals are generated by the connected Audio Device Codec.

In general, before establishing a voice call it is possible to select one of the two configurations and in accordance with the selected setting, configure the module and the codec via the AT commands provided by Telit, refer to documents [3]. The next pages describe the use of these AT commands.

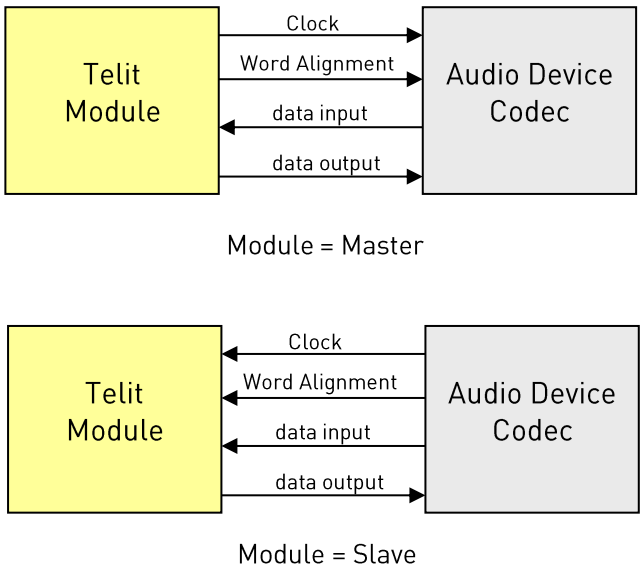

fig. 2: Master and Slave Configurations

4. DVI AT Commands

Several DVI audio bus configurations are available via AT#DVI and AT#DVIEXT commands. The tables in the following sub-sections summarize their parameters; refer to documents [3] for AT commands syntax details.

4.1. AT#DVI

AT#DVI command enables/disables the DVI interface, selects the DVI port, and sets the module in Master or Slave configuration. The following table shows the AT command parameters values.

AT#DVI =<mode>,<dviport>,<clockmode>		
<mode>	<dviport>	<clockmode>
0 → disable DVI interface, factory setting for UE910 products 1 → enable DVI interface, factory setting for HE901 and UL865 products 2 → reserved	1 → reserved 2 → select DVI port 2	0 → DVI slave 1 → DVI master, factory setting

Tab. 2: DVI Configuration via AT#DVI command

4.2. AT#DVIEXT

AT#DVIEXT command sets the module in Normal or Burst DVI Audio Format:

- In Normal DVI Audio Format the WAO signal defines the left and right audio channel.
- In Burst DVI Audio Format the WAO signal defines the beginning of the audio frame.

The following table shows the AT command parameters values.

DVI Audio Format (Mode)	AT#DVIEXT <config>,<samplerate>,<samplewidth>,<audiomode>,<edge>				
	<config>	<samplerate>	<samplewidth> bit per sample	<audiomode>	<edge>
Normal (I^2S)	1 factory setting	0 → 8 [KHz], factory setting 1 → 16 [KHz]	0 → 16 bits per sample factory setting 1 → 18 bits per sample 2 → 20 bits per sample 3 → 24 bits per sample 4 → 32 bits per sample	0 → Mono 1 → Dual Mono In Dual Mono the same Data Word is transmitted on both audio channels (right and left). Factory setting.	0 → the falling edge of the clock is used to shift out the next data to transmit. The received data bit is captured on the rising edge of the clock, factory setting. 1 → reserved
Burst (PCM)	0				0 → the falling edge of the clock is used to shift out the next data to transmit. The received data bit is captured on the rising edge of the clock. 1 → the rising edge of the clock is used to shift out the next data to transmit. The received data bit is captured on the falling edge of the clock.

Tab. 3: DVI Audio Format configuration via AT#DVIEXT command

5. DVI Setting Examples

The next chapters show examples concerning the audio formats provided by the DVI audio bus in Master and Slave configurations. All the following setting examples are performed using the hardware configuration shown in fig. 3. I²C bus is used to configure the MAX9867 Codec[2] [2]: the user by means of suitable AT commands can control the codec. The DVI bus provides the voice connection between the two devices.

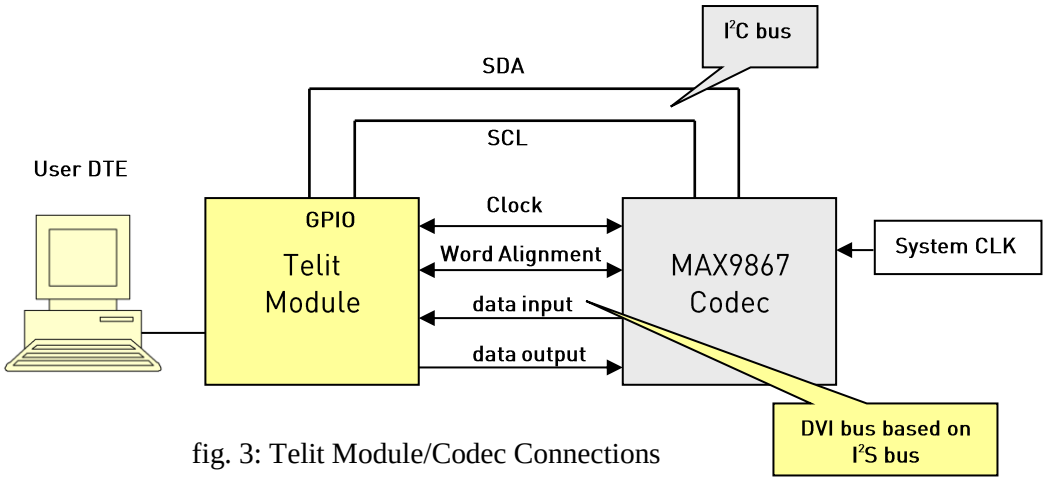

fig. 3: Telit Module/Codec Connections

The setting examples are organized as shown in the figure below.

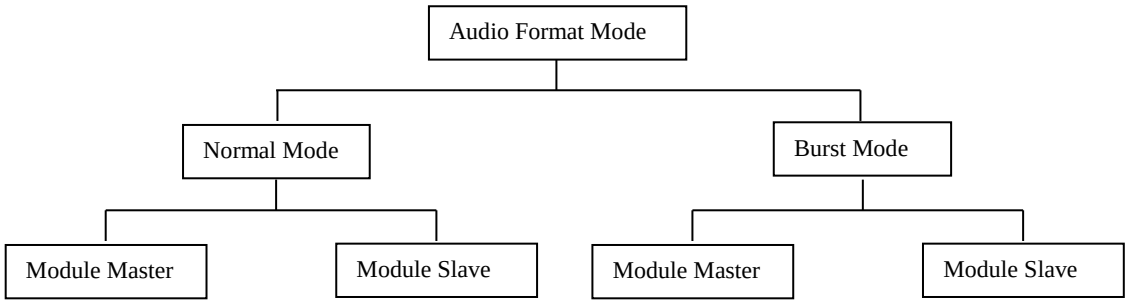

fig. 4: DVI Configurations

[2] The following examples use the MAX9867 Codec, see chapter 6.2 for a schematic reference design. In general, the user can use any codec compliant with the technical requirements of the Telit's modules.

5.1. Normal Mode (I^2S)

5.1.1. Module is Master

The

fig. **5** shows a timing diagram that refers to the module in the role of master. In this case, WAO and CLK signals are generated by the module. The WAO signal defines the frame of the two audio channels: left and right.

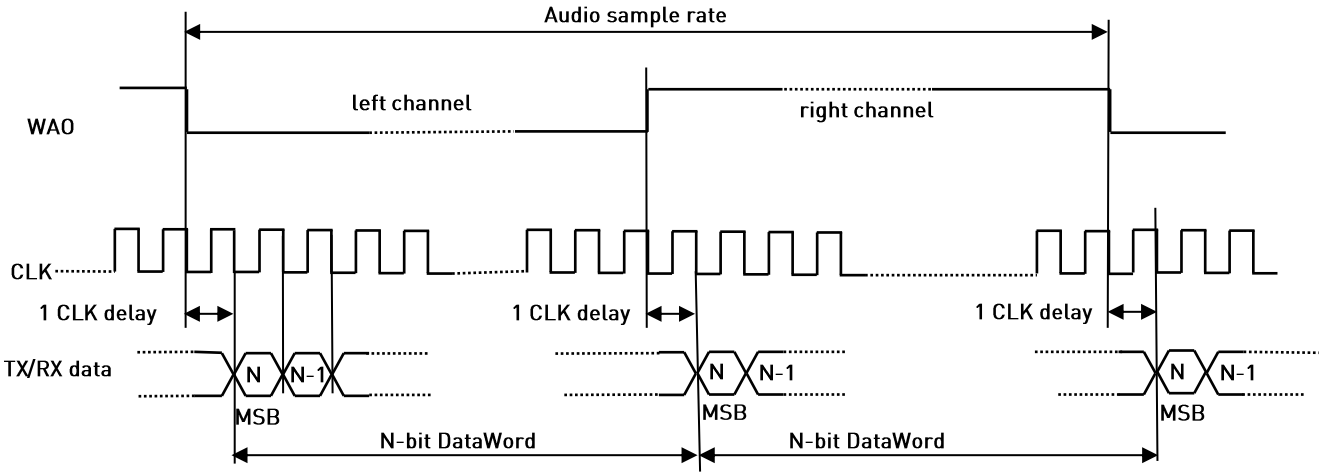

fig. 5: Module is Master/Normal mode/N bits per sample/Dual Mono

When module is Master the BitClockFrequency (CLK) is provided by the following expression:

$$BitClockFrequency = DataWordBit \times ChannelNumber \times AudioSampleRate$$

Refer to Tab. 4 for the BitClockFrequency generated by the Module.

<samplewidth>	DataWordBit	Audio channels	AudioSampleRate	
			8 KHz	16 KHz
			BitClockFrequency in KHz	
0	16	2	256	512
1	18	2	384[3]	768
2	20	2		
3	24	2		
4	32	2	512	1024

Tab. 4: BitClockFrequency generated by the module in Master/Normal Mode

[3] The module generates 384 or 768 KHz also when the audio sample has 16 or 20 bits. In these configurations only 16 or 20 bits are taken in consideration, all other bits must be discarded.

Here are the lists of AT commands used to set the module in Master Normal (I^2S) Mode, and configure the codec in accordance with the module setting. After each command is described the uses parameters values meaning.

Configure the Module in Master Normal (I^2S) Mode

DVI bus

AT#DVI=1,2,1
OK

1 enable DVI interface
2 use DVI port 2 (mandatory)
1 set the module as Master (factory setting)

AT#DVIEXT=1,0,0,1,0
OK

1 Normal Mode (factory setting)
0 sample rate 8 KHz (factory setting)
0 16 bits per sample (factory setting)
1 Dual Mono, the same Data Word is transmitted on both audio channels (factory setting)
0 the falling edge of the clock is used to shift out the next data to transmit;
the received data bit is captured on the rising edge of the clock. (factory setting)

Configure the codec in Slave Normal (I^2S) Mode

I^2C bus

AT#I2CWR=X,Y,30,4,19
>00109000100A330000330C0C09092424400060
OK

X GPIO number used as SDA, refer to [3]
Y GPIO number used as SCL, refer to [3]
30 Device address on I^2C, refer to [2]
4 Register address from which start the writing, refer to [2]
19 number of bytes to write
>00109000…..refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA, refer to [3]
Y GPIO number used as SCL, refer to [3]
30 Device address on I^2C, refer to [2]
17 Register address where write data, refer to [2]
1 number of bytes to write
>8A, refer to [2]

The fig. 6 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (256 KHz) and WAO signals are generated by the module.

Left channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

Right channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

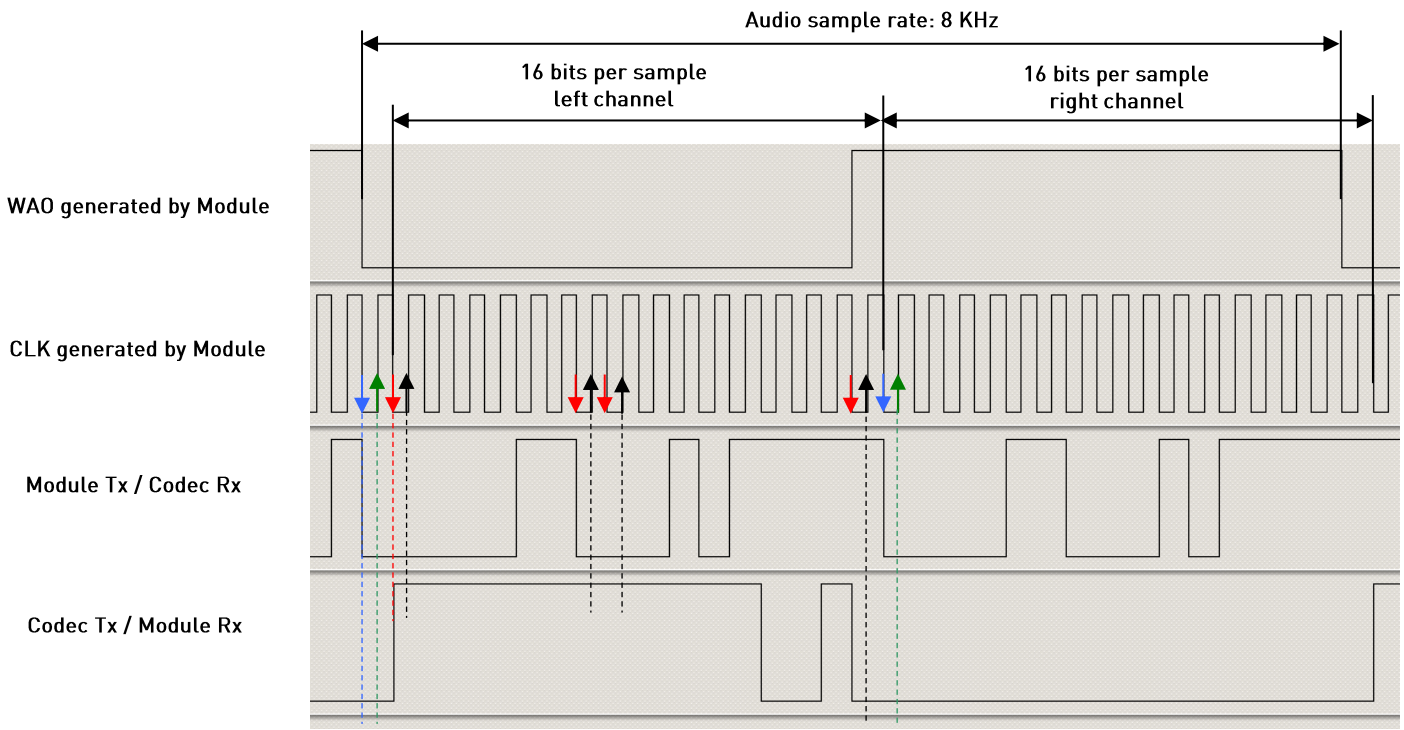

fig. 6: Module is Master/Normal Mode/16 bits per sample/Dual Mono/<edge>=0

5.1.2. Module is Slave

Here are the lists of the AT commands used to set the module in Slave Normal (I^2S) Mode, and configure the codec in accordance with the module setting. After each command is described the used parameters values meaning.

Configure the module in Slave Normal (I^2S) Mode

DVI bus

AT#DVI=1,2,0
OK

1 enable DVI interface
2 use DVI port 2 (mandatory)
0 set the module as Slave

AT#DVIEXT=1,0,3,1,0
OK

1 Normal Mode (factory setting)
0 sample rate 8 KHz (factory setting)
3 24 bits per sample
1 Dual Mono, the same Data Word is transmitted on both audio channels (factory setting)
0 the falling edge of the clock is used to shift out the next data to transmit;
the received data bit is captured on the rising edge of the clock. (factory setting)

Configure the codec in Master Normal (I^2S) Mode

I^2C bus

AT#I2CWR=X,Y,30,4,19
>00101000900233000033OC0C09092424400060
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
4 Register address from which start the writing
19 number of bytes to write
>00101000…..refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
17 Register address where write data
1 number of bytes to write
>8A, refer to [2]

NOTICE: *the codec is in Master configuration and generates a clock equal to 384 KHz. On the module the selected number of bits per sample is 24, see Tab. 4*

The fig. 7 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (384 KHz) and WAO signals are generated by the codec.

Left channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

Right channel:

↓: Data transitions occur on the falling edge of the CLK

↑: Data are latched on the rising edge of the CLK

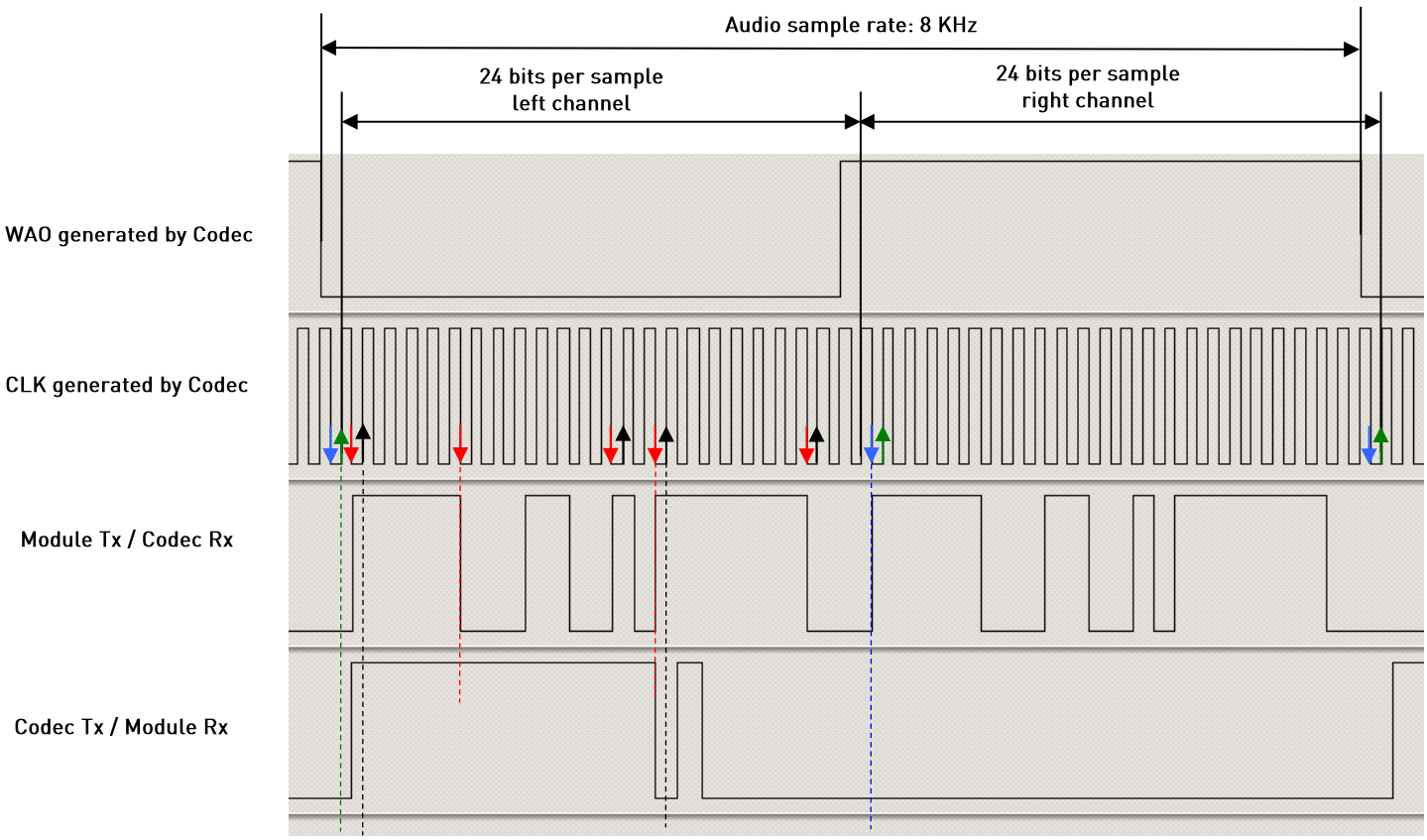

fig. 7: Module is Slave/Normal Mode/24 bits per sample/Dual Mono/<edge>=0

5.2. Burst Mode (PCM)

5.2.1. Module is Master

The fig. 8 shows a timing diagram that refers to the module in the role of master. In this case, the WAO and CLK signals are generated by the module. The WAO signal defines the frame of the audio channel.

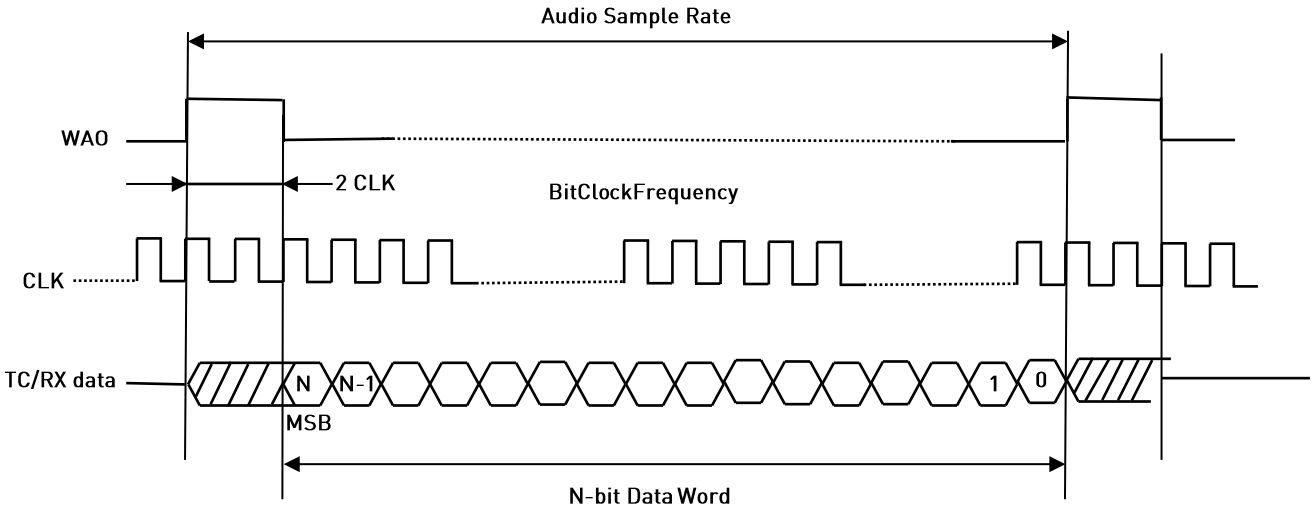

fig. 8: Module is Master/Burst mode/N bits per Sample/Mono Mode

When module is Master the BitClockFrequency (CLK) is provided by the following expression:

$$BitClockFrequency = (DataWordBit + 2) \times AudioSampleRate$$

Refer to Tab. 5 for the BitClockFrequency generated by the module in accordance with the connected MAX9867 codec used in the examples.

<samplewidth>	DataWordBit	AudioSampleRate	
		8 [KHz]	16 [KHz]
		BitClockFrequency [KHz]	
0	16 (+ 2[4])	144	288
4	32 (+ 2)	272	544

Tab. 5: BitClockFrequency in Burst Mode

[4] The width of the WAO pulse is 2 CLK.

Here are the lists of AT commands used to set the module in Master Burst (PCM) Mode, and configure the codec in accordance with the current module setting. After each command is described the used parameters values meaning.

Configure the module in Master Burst (PCM) Mode.

DVI bus

AT#DVI=1,2,1
OK

1 enable DVI
2 use DVI port 2 (mandatory)
1 DVI Master (factory setting)

AT#DVIEXT=0,0,0,0,1
OK

0 Burst Mode
0 sample rate 8 KHz (factory setting)
0 16 bits per sample (factory setting)
0 Mono Mode
1 the rising edge of the clock is used to shift out the next data to transmit, the received data bit is captured on the falling edge of the clock

Configure the codec in Slave Burst (PCM) Mode.

I^2C bus

AT#I2CWR=X,Y,30,4,19
> 00109000600A330000330C0C09092424400060

OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
4 Register address from which start the writing
19 number of bytes to write
>00109000…..refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
17 Register address where write data
1 number of bytes to write
>8A refer to [2]

The fig. 9 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (144 KHz) and WAO signals are generated by the module.

↑: Data transitions occur on the rising edge of the CLK

↓: Data are latched on the falling edge of the CLK

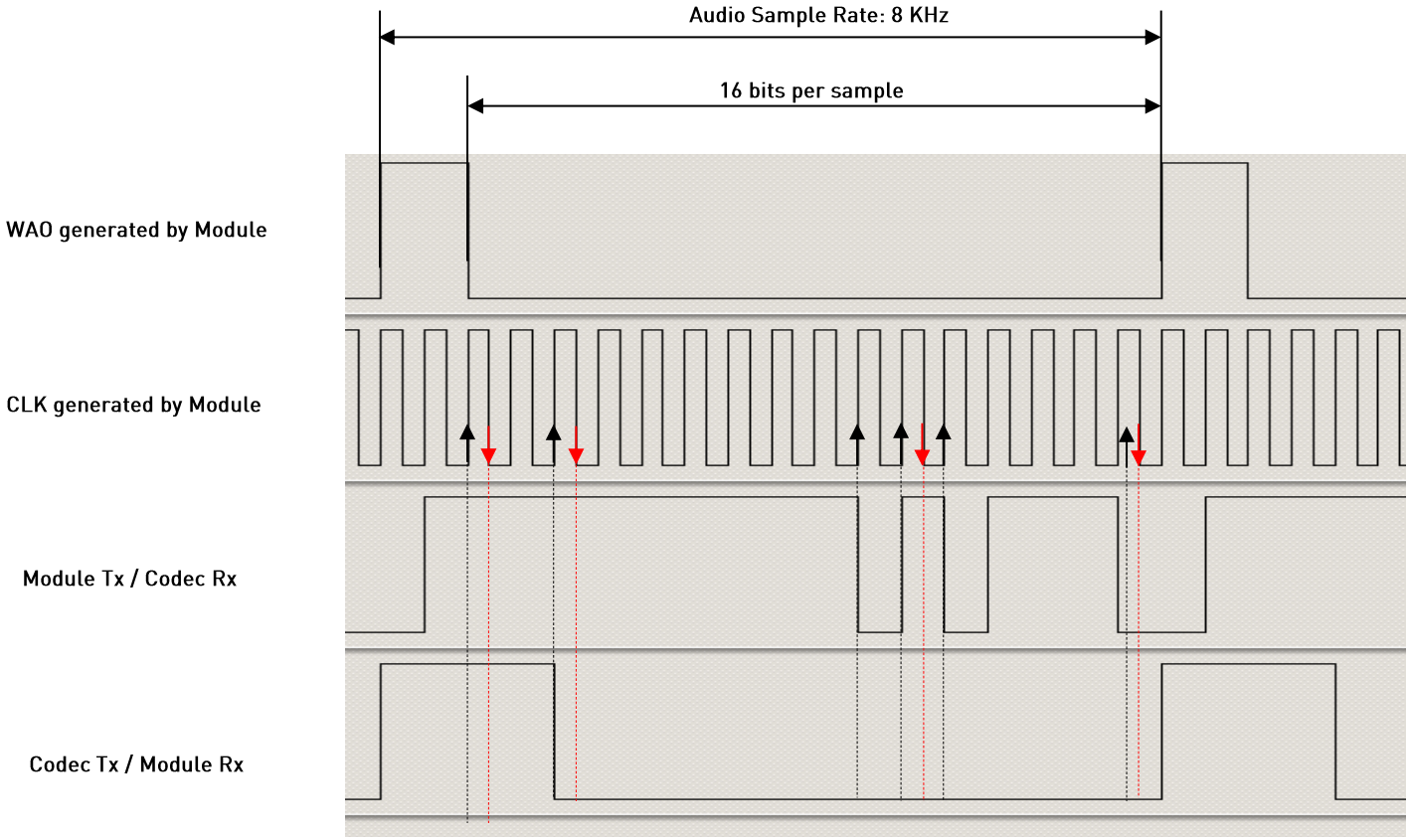

fig. 9: Module is Master/Burst Mode/16 bits per Sample/Mono Mode/<edge>=1

5.2.2. Module is Slave

The fig. 10 shows a timing diagram that refers to the codec in master configuration. In this case, the WAO and CLK signals are generated by the codec.

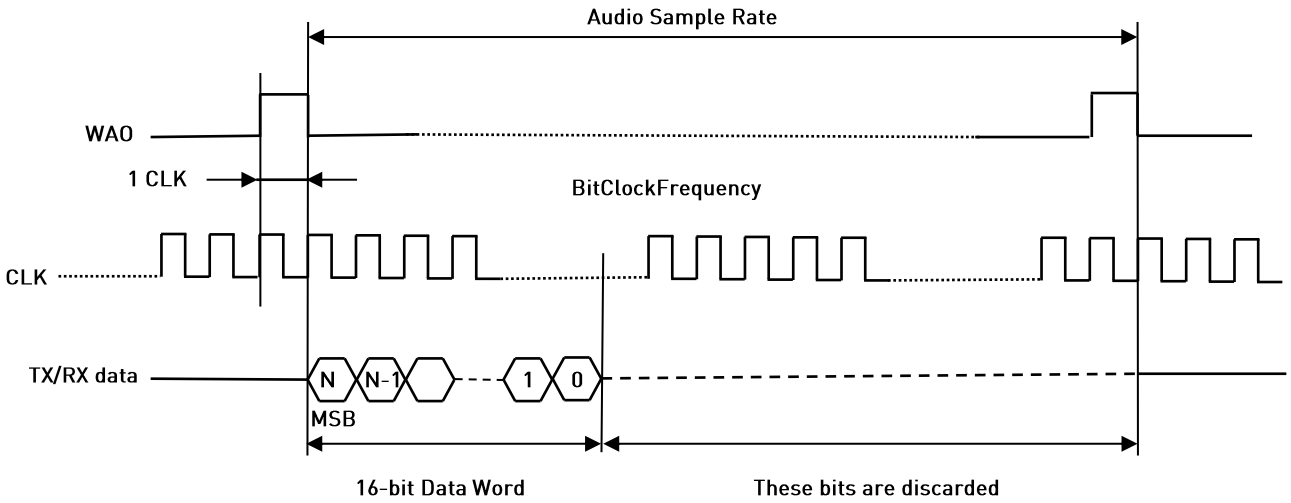

fig. 10: Module is Slave/Burst Mode/N bits per Sample/Mono Mode

Here are the lists of AT commands used to set the module in Slave Burst (PCM) Mode, and configure the codec in accordance with the current module setting. After each command is described the used parameters values meaning.

Configure the module in Slave Burst (PCM) Mode.

DVI bus

AT#DVI=1,2,0
OK

1 enable DVI interface
2 use DVI port 2 (mandatory)
0 set the module as Slave

AT#DVIEXT=0,0,0,0,1
OK

0 Burst Mode
0 sample rate 8 KHz (factory setting)
0 16 bits per sample (factory setting)
0 Mono Mode
1 the rising edge of the clock is used to shift out the next data to transmit, the received data bit is captured on the falling edge of the clock

Configure the codec in Master Burst (PCM) Mode.

I^2C bus

AT#I2CWR=X,Y,30,4,19
> 00101000A40A330000330C0C09092424400060
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
4 Register address from which start the writing
19 number of bytes to write
>00101000…..refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X GPIO number used as SDA
Y GPIO number used as SCL
30 Device address on I^2C
17 Register address where write data
1 number of bytes to write
>8A refer to [2]

The fig. 11 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (384 KHz) and WAO signals are generated by the codec.

↑: Data transitions occur on the rising edge of the CLK

↓: Data are latched on the falling edge of the CLK

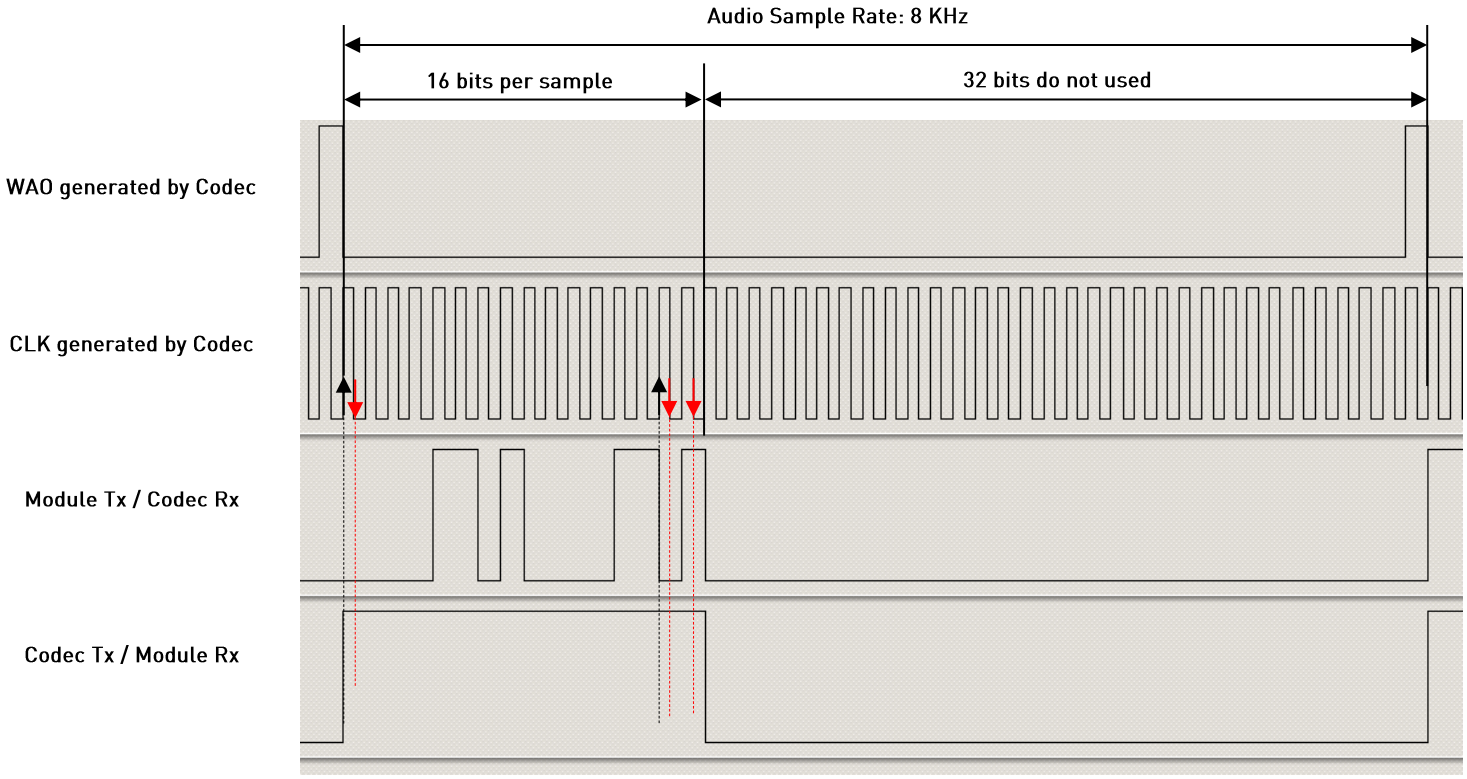

fig. 11: Module is Slave/Burst Mode/16 bits per Sample/Mono Mode/<edge>=1

6. Annex

6.1. I²S Overview

This chapter provides a short description of the standard I2S bus. This standard suitably modified is used by the DVI interface implemented on the Telit's modules.

The standard I2S is an electrical serial bus designed for connecting digital audio devices. This popular serial bus has been developed by Philips® in 1986 as a 3-wire bus for interfacing to audio chips such as codecs. It is a simple data interface, without any form of address or device selection.

Refer to fig. 12: the I2S design handles audio data separately from clock signals. On an I2S bus, there is only one bus master and one transmitter.

In high-quality audio applications involving a Codec, the Codec is typically the master so that it has precise control over the I2S bus clock.

An I2S bus design consists of the following serial bus lines:

- SD: Serial Data
- WS: Word Select
- Serial Clock: SCK

The I2S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.

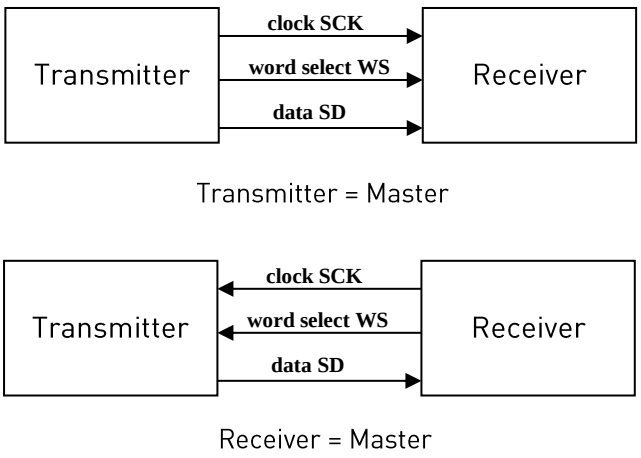

fig. 12: I²S bus configurations

6.2. Schematic

A schematic example of an interface between the Telit's modules and the MAX9867 CODEC could be the following:

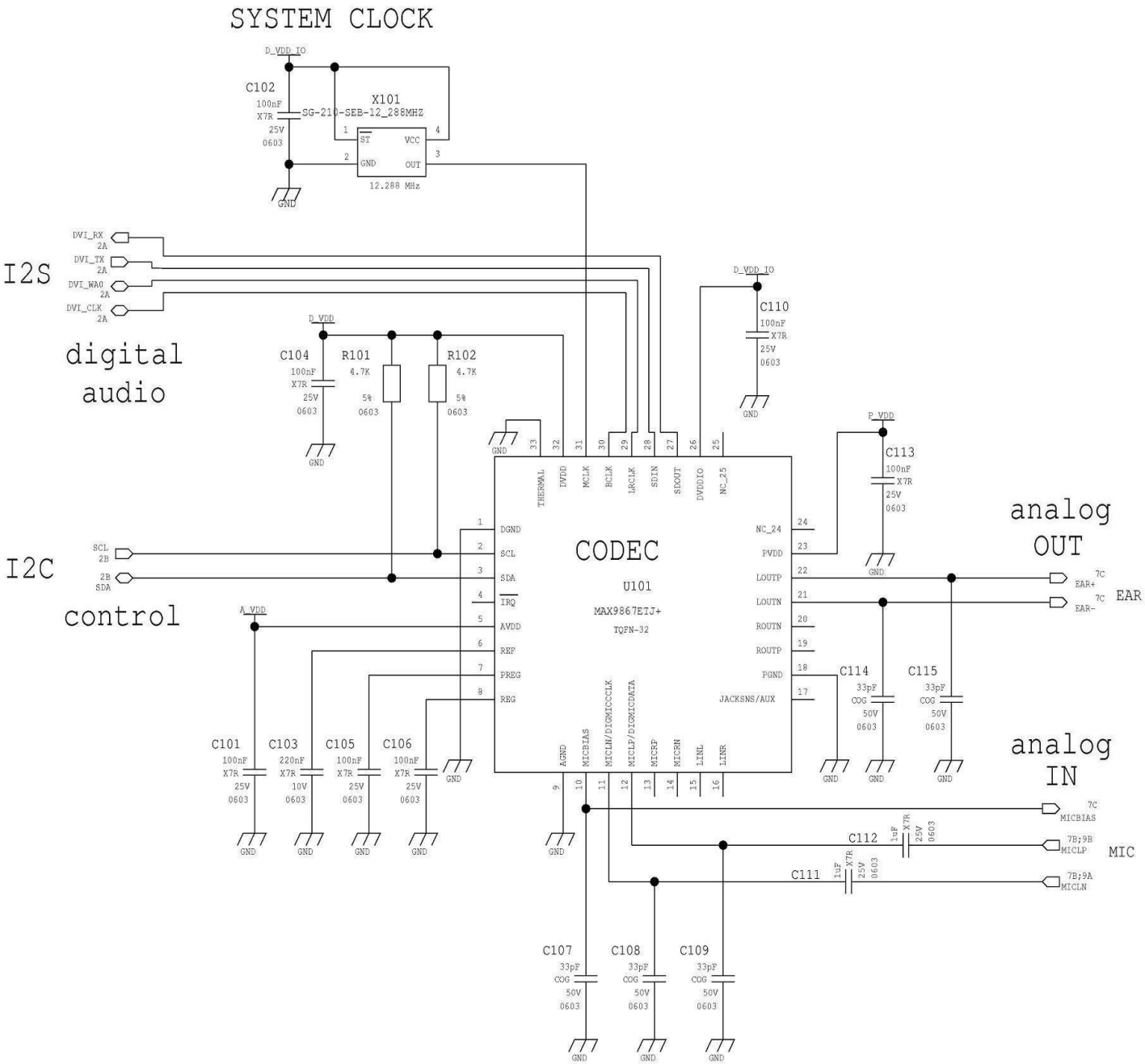

fig. 13: Schematic for Reference Design