LE866 DIGITAL VOICE INTERFACE APPLICATION NOTE

APPLICABILITY TABLE

PRODUCTS

LE866-SV1	SW VER.: 23.00.003

NOTE:

The features described in the present document are provided by the products equipped with the software versions equal or higher than the versions shown in the table. See also the Document History chapter.

DISCLAIMER

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CONTENTS

1 INTRODUCTION

1.1 Scope

The present document provides the reader with a guideline concerning the setting and use of the Digital Voice Interface developed on the Telit's LE866 modules shown in the Applicability Table.
This Application Note covers the configurations of the Digital Voice Interface, e.g.: the selections of the voice sampling frequency, the bit number of the voice sample, the audio formats, etc. In addition, the document shows some configurations of a popular Audio Codec connected to the module. These activities are accomplished via I2S and I2C buses; the hardware characteristics of the two buses are beyond the scope of the document.

1.2 Audience

The document is intended for those users that need to develop applications dealing with signal voice in digital format.

1.3 Contact Information, Support

For general contact, technical support services, technical questions and report documentation errors contact Telit Technical Support at:

TS-EMEA@telit.com

TS-AMERICAS@telit.com

TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/support

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.
Telit appreciates feedback from the users of our information.

1.4 List of acronyms

Acronym	Description
TTSC	Telit Technical Support Centre
USB	Universal Serial Bus
DVI	Digital Voice Interface
DTE	Data Terminal Equipment
LTE	Long Term Evolution
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
MSB	Most Significant Bit
SIM	Subscriber Identification Module
ADC	Analog – Digital Converter
DAC	Digital – Analog Converter
I/O	Input Output
GPIO	General Purpose Input Output
CMOS	Complementary Metal – Oxide Semiconductor
CLK	Clock
CS	Chip Select
RTC	Real Time Clock
PCB	Printed Circuit Board
ESR	Equivalent Series Resistance
VSWR	Voltage Standing Wave Radio
VNA	Vector Network Analyzer

1.5 Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

1.6. Related Documents

- LE866 HW User Guide 1VV0301210
- LE866 AT Commands Reference Guide 80471ST10691A
- Telit EVK2 User Guide 1vv0300704
- MAX9867 Ultra-Low Power Stereo Audio Codec documentation ref to MAXIM

2 OVERVIEW

The aim of this document is the description of some hardware solutions useful for developing a product with the Telit LE866 module.
In this document all the basic functions of a mobile phone will be taken into account; for each one of them a proper hardware solution will be suggested and eventually the wrong solutions and common errors to be avoided will be evidenced. Obviously this document cannot embrace the whole hardware solutions and products that may be designed. The wrong solutions to be avoided shall be considered as mandatory, while the suggested hardware configurations shall not be considered mandatory, instead the information given shall be used as a guide and a starting point for properly developing your product with the Telit LE866 module. For further hardware details that may not be explained in this document refer to the Telit LE866 Product Description document where all the hardware information is reported.

NOTICE:
(EN) The integration of the LTE **LE866** cellular module within user application shall be done according to the design rules described in this manual.

(IT) L'integrazione del modulo cellulare LTE **LE866** all'interno dell'applicazione dell'utente dovrà rispettare le indicazioni progettuali descritte in questo manuale.

(DE) Die Integration des **LE866** LTE Mobilfunk-Moduls in ein Gerät muß gemäß der in diesem Dokument beschriebenen Kunstruktionsregeln erfolgen.

(SL) Integracija LTE **LE866** modula v uporabniški aplikaciji bo morala upoštevati projektna navodila, opisana v tem priročniku.

(SP) La utilización del modulo LTE **LE866** debe ser conforme a los usos para los cuales ha sido deseñado descritos en este manual del usuario.

(FR) L'intégration du module cellulaire LTE **LE866** dans l'application de l'utilisateur sera faite selon les règles de conception décrites dans ce manuel.

(HE) האינטגרטור מתבקש ליישם את ההנחיות המפורטות במסמך זה בתהליך האינטגרציה של המודם הסלולרי עם המוצר. **LE866**

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3 DVI OVERVIEW

Before dealing with the configuration and technical aspects of the Telit's Digital Voice Interface (DVI) it is useful to illustrate briefly how this interface can be used, refer to fig. 1.

The voice coming from the downlink, in digital format, is captured by the dedicated software running on the Telit's module and directed to the Digital Voice Interface. The Audio Codec decodes the voice and sends it to the speaker. The voice captured by the microphone is coded by the Audio Codec and directed through the Digital Voice Interface to the module that collects the received voice, in digital format, and sends it on the uplink.

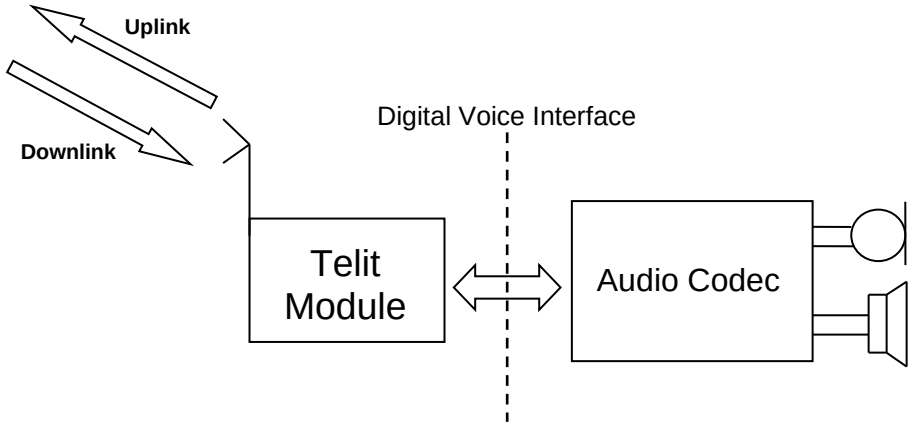


fig. 1: Example of Digital Voice Interface Use

NOTE:
The Digital Voice Interface supports the Echo canceller functionality, which is beyond the scope of the present document. Refer to the AT Commands specification for the specific AT commands.

4 DVI BUS

4.1 DVI PIN LIST

The physical DVI interface provided by the Telit's modules is based on the standard I2S Bus.
An overview of the standard I2S Bus is described in chapter 6.1.
The following Table summarizes the DVI signals and a short description for each one of them; refer to Telit Hardware User Guide, in accordance with the used module, to have information on electrical characteristics and signals pin-out.

Signal	Function	Description
DVI_CLK	Clock	Data Clock
DVI_WAO	Word Alignment	Frame Synchronism
DVI_RX	Serial audio data input	Received Data
DVI_TX	Serial audio data output	Transmitted Data

The figures below show the two configurations of the DVI interface relating to the Word Alignment and Clock signals. When the module is Master the Clock and Word Alignment signals (also called Word Alignment Output WAO) are generated by the module itself, otherwise, when it is Slave, both signals are generated by the connected Audio Device Codec.
In general, before establishing a voice call it is possible to select one of the two configurations and in accordance with the selected setting, configure the module and the codec via the AT commands described in At User Guide.
The next pages describe the use of these AT commands.

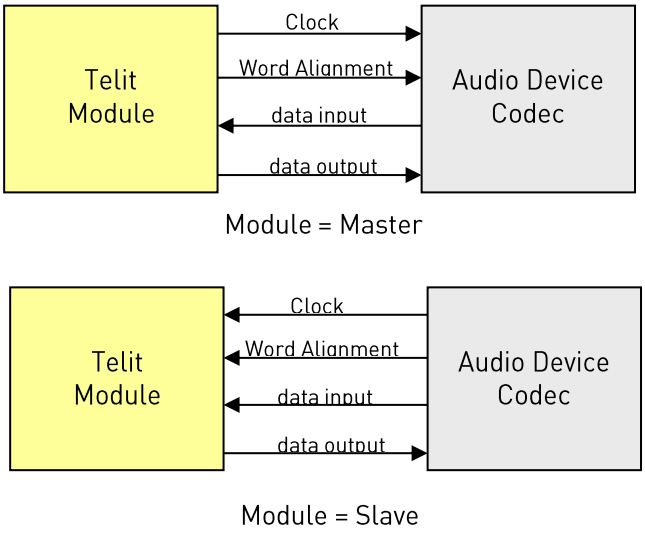


fig. 2: Master and Slave Configurations

5 DVI AT COMMANDS

Several DVI audio bus configurations are available via AT#DVI and AT#DVIEXT commands.
The tables in the following sub-sections summarize their parameters; refer to the AT Commands User Guide for the syntax details.

5.1 AT#DVI

The DVI signals are Alternate functions of GPIOs 1, 2, 3 and 4.
The AT#DVI command enables/disables the DVI interface, selects the DVI port, and sets the module in Master or Slave configuration. The table below shows the AT command parameters values.

AT#DVI =<mode>,<dviport>,<clockmode>

<mode>	<dviport>	<clockmode>
0: disable DVI interface, factory setting 1: enable DVI interface 2: reserved	2: select DVI port 2, factory setting	0: DVI slave 1: DVI master, factory setting

NOTE:
<mode> =2 and <clockmode>=0 not supported on LE866

5.2 AT#DVIEXT

AT#DVIEXT command sets the module in Normal or Burst DVI Audio Format:

- In Normal DVI Audio Format the WAO signal defines the left and right audio channel.
- In Burst DVI Audio Format the WAO signal defines the beginning of the audio frame.

The following table shows the AT command parameters values.

AT#DVIEXT <config>,<samplerate>,<samplewidth>,<audiomode>,<edge>					
DVI Audio Format (mode)	**<config>**	**<samplerate>**	**<samplewidth>**	**<audiomode>**	**<edge>**
Normal (I2S)	1(factory setting)	0: 8 [KHz] sample rate 1: 16 [KHz] sample rate	0: 8 bits per sample 1: 16 bits per sample	0: Mono Mode	0: data is transmitted on the falling edge of the clock and sampled on its rising edge, factory setting. 1: data is transmitted on the rising edge of the clock and sampled on its falling edge.
Burst (PCM)	0	0: 8 [KHz] sample rate factory setting 1: 16 [KHz] sample rate	0: 8 bits per sample 1: 16 bit per sample	0	don't care if the <edge> value is 1 or 0, data is always transmitted on the rising edge of the clock and sampled on its falling edge

Tab. 1: DVI Audio Format configuration via AT#DVIEXT command

NOTE:

The preferred setting for LE866 is AT#DVIEXT=1,1,1

Please avoid using #DVIEXT command when a call is active

6 DVI SETTING EXAMPLES

The next chapters show examples concerning the audio formats supported by the DVI audio bus in Master and Slave configurations. All the following setting examples are performed using the hardware configuration shown in fig. 3. I2C bus is used to configure the MAX9867 Codec: the user by means of AT commands can control the codec. The DVI bus provides the voice connection between the two devices.

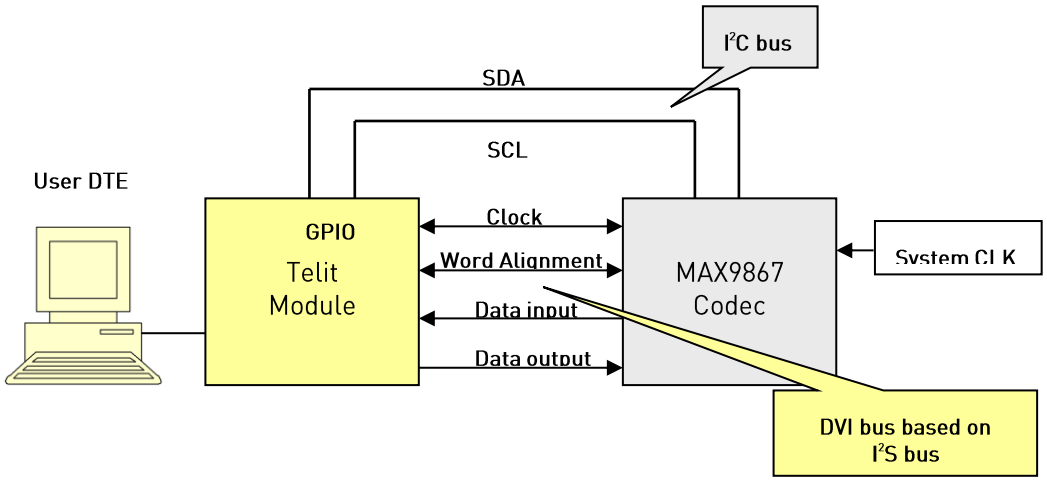


fig. 3: Telit Module/Codec Connections

The setting examples are organized as shown in the figure below.

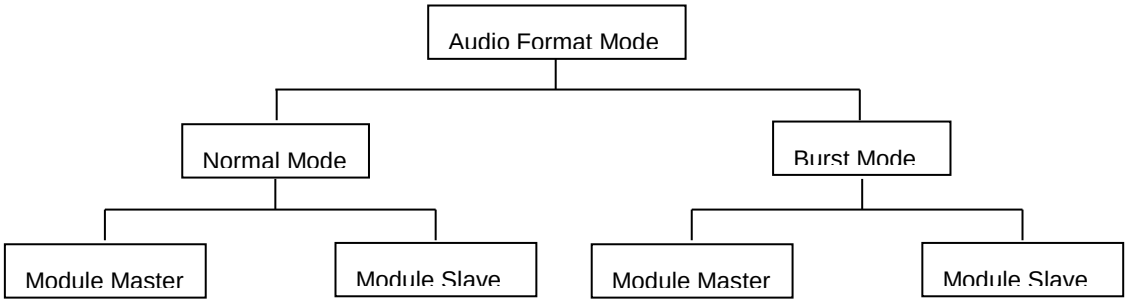


fig. 4: DVI Configurations

NOTE:
The examples use the MAX9867 Codec, see chapter 6.2 for a schematic reference design. In general, the user can use any codec compliant with the technical requirements of the used module.

6.1 Normal (I2S) Mode

6.1.1 Module is Master

In this configuration the WAO and CLK signals are generated by the module. The WAO signal defines the frame of the two audio channels: left and right, refer to fig. 5. The BitClockFrequency (CLK) is provided by the following expression:

$$BitClockFrequency = DataWordBit \times ChannelNumber \times AudioSampleRate$$

The BitClockFrequency values are shown in Tab. 4.

			AudioSampleRate	
<samplewidth>	DataWordBit	Audio Channels	8 KHz	16 KHz
			BitClockFrequency in KHz	
0	8	2	128	256
1	16	2	256	512

Tab. 2: BitClockFrequency generated by the module in Master/Normal Mode

Here are the lists of AT commands used to set the module in Master/Normal (I2S) Mode, and configure the codec in accordance with the module setting. The meanings of the used parameters values are described after each command

Configure the module in Master/Normal (I2S) Mode (DVI Bus)

AT#DVI=1,2,1
OK

1 enable DVI interface
2 use DVI port 2
1 set the module as Master (factory setting)

Setting for BitClockFrequency = 512 KHz

AT#DVIEXT=1,1,1,0,0
OK

1 Normal Mode
1 sample rate 16 KHz
1 16 bits per sample
0 Mono
0 data is transmitted on the falling edge of clock and sampled on the rising edge

Configure the codec in Slave/Normal (I2S) Mode (I2C Bus)

AT#I2CWR=X,Y,30,4,19

>00109000100A330000330C0C09092424400060

OK

X GPIO number used as SDA, refer to AT User Guide

Y GPIO number used as SCL, refer to AT User Guide

30 Device address on I2C, refer to MAX9867 documentation

4 Register address from which start the writing, refer to MAX9867 documentation

19 number of bytes to write

>00109000….. refer to MAX9867 documentation

AT#I2CWR=X,Y,30,17,1

>8A

OK

X GPIO number used as SDA, refer to AT User Guide

Y GPIO number used as SCL, refer to AT User Guide

30 Device address on I2C, refer to MAX9867 documentation

17 Register address where write data, refer to MAX9867 documentation

1 number of bytes to write

>8A refer to MAX9867 documentation

The fig. 5 shows the screenshot of the timing diagram, captured by a logic analyzer, using the above described module/codec setting. The CLK (512 KHz) and WAO signals are generated by the module, data is transmitted on the rising edge of clock and sampled on the falling edge.

Left channel:

: Data transitions occur on the rising edge of the CLK

: Data are latched on the falling edge of the CLK

Right channel:

: Data transitions occur on the rising edge of the CLK

: Data are latched on the falling edge of the CLK

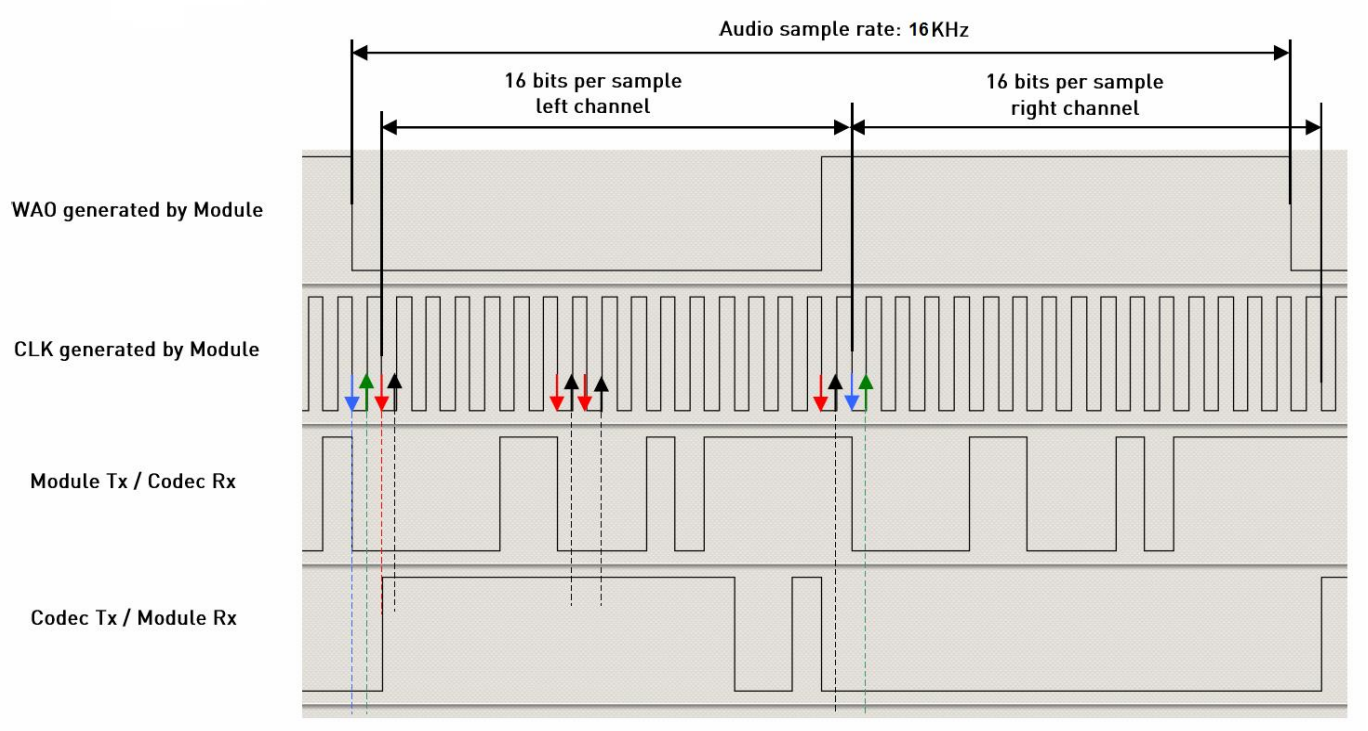


fig. 3: Module is Master/Normal mode/16 bits per sample/Mono/<edge> = 0

7 ANNEX

7.1 I²S Bus Overview

This chapter provides a short description of the standard I2S bus. This standard suitably modified is used by the DVI interface implemented on the Telit modules.

The standard I2S is an electrical serial bus designed for connecting digital audio devices. This popular serial bus has been developed by Philips® in 1986 as a 3-wire bus for interfacing to audio chips such as codecs. It is a simple data interface, without any form of address or device selection.

Refer to fig. 9: the I2S design handles audio data separately from clock signals. On an I2S bus, there is only one bus master and one transmitter.

In high-quality audio applications involving a codec, the codec is typically the master so that it has precise control over the I2S bus clock.

An I2S bus design consists of the following serial bus lines:

- SD: Serial Data
- WS: Word Select
- Serial Clock: SCK

The I2S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.

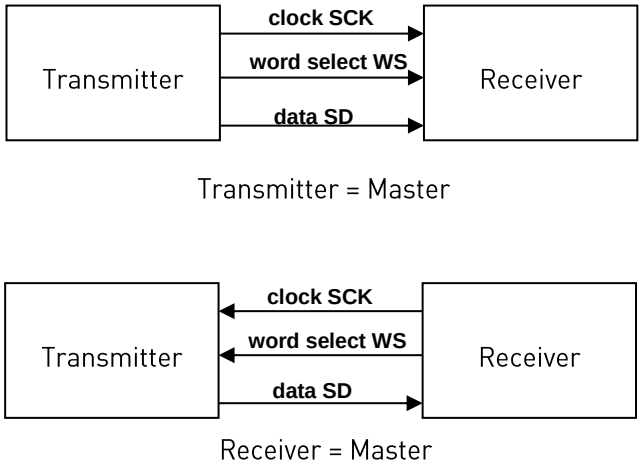
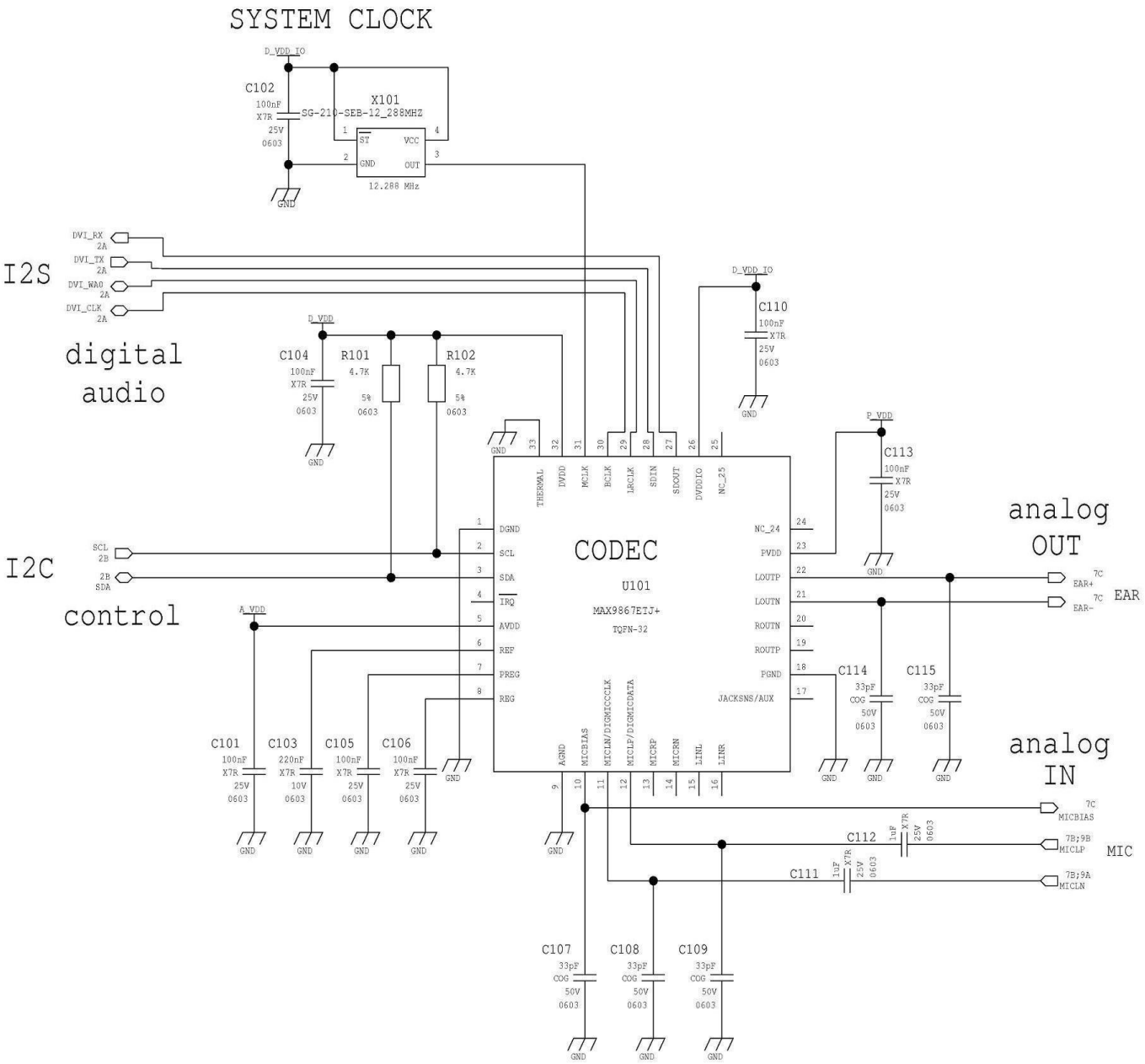


fig. 4: I2S Bus Configurations

7.2 Schematic

A schematic example of an interface between a Telit Module and the MAX9867 Codec could be the following:



8 DOCUMENT HISTORY

8.1 Revisions

Revision	Date	Changes
0	2017-01-16	Initial Version


Design Review
120°
180°
Process
Validation
240°
RF/EMC Pre-Certification
Module Selection
60°
300°
Approvals
Support
360°
Value Added Services & Connectivity
Enterprise Integration &
Application Enablement
m2mair