LE910/LE920 Digital Voice Interface Application Note

80000NT11246A Rev. 3 – 2014-24-11

APPLICABILITY TABLE

	SW Versions
LE910 Family	**17.00.5x3**
LE910-EUG	
LE910-NAG	
LE910-NVG	
LE920 Family	
LE920-EUG	
LE920-NAG	

Note: the features described by the present document are provided by the products equipped with the software versions equal or higher than the versions shown in the table.

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Contents

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Figures

Tables

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1. Introduction

The present document provides the reader with a guideline concerning the setting and use of the Digital Voice Interface developed on the Telit's modules families shown in the Applicability Table.

1.1. Scope

This Application Note covers the configurations of the Digital Voice Interface, e.g.: the selections of the voice sampling frequency, the bit number of the voice sample, the audio formats, etc. In addition, the document shows some configurations of a popular Audio Codec connected to the Module. These activities are accomplished via I^2S and I^2C buses; the hardware characteristics of the two buses are beyond the scope of the document.

1.2. Audience

The document is intended for those users that need to develop applications dealing with signal voice in digital format.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit Modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit Technical Support Center (TTSC).
Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.
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1.4. Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "Overview" provides an overview of the document.

Chapter 3: "Module's DVI (PCM)" describes the DVI port

Chapter 4: "Protocol description"

Chapter 5: "Parameters and timing characteristics"

Chapter 6: "Custom AT commands"

Chapter 7: "External codec" provides an example of interfacing with an external audio codec.

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

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1.6. Related Documents

[1] LE910 Hardware User Guide, 1vv0301089
[2] MAX9867 Ultra-Low Power Stereo Audio Codec, MAXIM
[3] LE910 AT Commands Reference Guide, 80421ST10585A
[4] LE920 Hardware User Guide, 1vv0301026
[5] LE920 AT Commands Reference Guide, 80407ST10116A

1.7. Document History

Revision	Date	Changes
0	2014-03-31	First issue
1	2014-08-08	Updated supported modes
2	2014-08-22	Updated supported modes Added note on CODEC example applicability
3	2014-11-09	Add LE920 support Updated DVI command setting

1.8. Abbreviations and Acronyms

DTE Data Terminal Equipment
DVI Digital Voice Interface
GPIO General Purpose Input/Output
I^2C Inter-Integrated Circuit
I^2S Inter-IC Sound
MSB Most Significant Bit

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2. Digital Voice Interface Use

Before dealing with the configuration and technical aspects of the Telit' Digital Voice Interface (DVI) it is useful to illustrate briefly where and how this interface can be used, refer to fig. 1

The voice coming from the downlink, in digital format, is captured by the dedicated software running on the Telit's module and directed to the Digital Voice Interface. The Audio Codec decodes the voice and sends it to the speaker. The other way round the voice captured by the microphone is coded by the Audio Codec and directed through the Digital Voice Interface to the module that collects the received voice, in digital format, and sends it on the uplink.
The **DVI** uses the PCM interface as part of the audio front end.

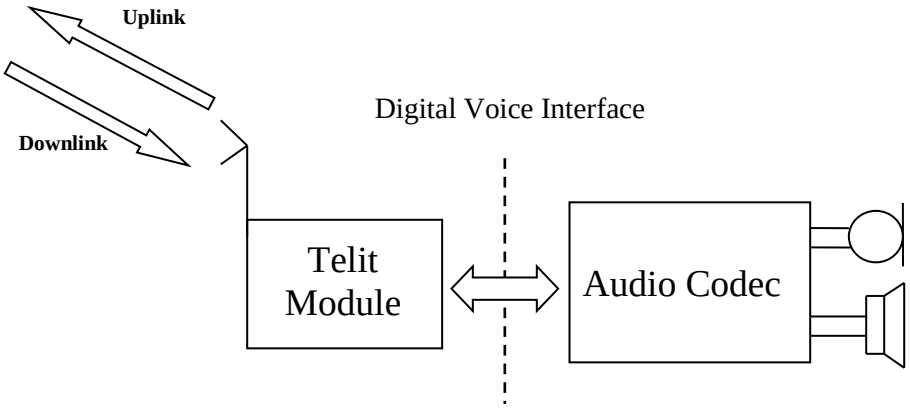

fig. 1: Example of Digital Voice Interface Use

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2.1. DVI Introduction

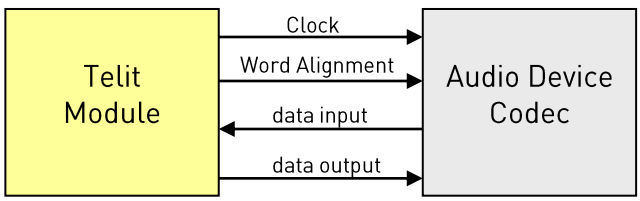
Although analog communication is ideal for human communication, analog transmission is neither robust nor efficient at recovering from line noise.
As example in the early telephony network, when analog transmission was passed through amplifiers to boost the signal, not only was the voice boosted but the line noise was amplified, as well. This line noise resulted in an often-unusable connection.
It is much easier for digital samples, which are comprised of 1 and 0 bits, in order to be separated from line noise. Therefore, when analog signals are regenerated as digital samples, a clean sound is maintained.
PCM converts analog sounds into digital form by sampling the analog sounds 8000 times per second and converting each sample into a numeric code. If you sample an analog signal at twice the rate of the highest frequency of interest, you can accurately reconstruct that signal back into its analog form (Nyquist theorem). Because most speech content is below 4000Hz, a sampling rate of 8000 times per second (8 KHz that means 125 µSec between samples) is required.

The physical DVI interface provided by the Telit's modules is based on the I^2S Bus. An overview of the standard I^2S Bus is described in chapter 4.1. Tab. 1 summarizes the DVI signals and a short description for each one of them: refer to documents [1] and [4] to have information on electrical characteristics and signals pin-out in accordance with the used module.

DVI Signal	DVI Signal name	Description
Clock	DVI_CLK	Data Clock
Word Alignment	DVI_WAO	Frame Synchronism
serial audio data input	DVI_RX	Received Data
serial audio data output	DVI_TX	Transmitted Data

Tab. 1: DVI Signals

The LE910 is supporting only the MASTER Mode.
The figures below show the configuration of the DVI interface relating to the Word Alignment and Clock signals. When the module is Master the Clock and Word Alignment signals (also called Word Alignment Output WAO) are generated by the module itself.



Module = Master

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2.2. DVI Configurations

The command AT#DVICFG is usable to configure the DVI interface.
Its syntax is the following:

#DVICFG – DVI CONFIGURATION	
AT#DVICFG=[<clock>[,<decoder pad>[,<decoder format>[, <encoder pad>[,<encoder format>]]]]]	Set command sets the DVI configuration Parameter: <**clock**>: Clock speed for master mode 0 : normal mode(factory default) 1 : high speed mode <**decoder pad**>: PCM padding enable in decoder path 0 : disable 1 : enable(factory default) <**decoder format**>: PCM format in decoder path 0 : u-Law 1 : A-Law 2 : linear(factory default) <**encoder pad**>: PCM padding enable in encoder path 0 : disable 1 : enable(factory default) <**encoder format**>: PCM format in encoder path 0 : u-Law 1 : A-Law 2 : linear(factory default) **Note**: • #DVICFG parameters are saved in the extended profile . • LE910 supports only the first parameter <**clock**> Normal mode (factory default) = 128KHz with sample rate 8k. High speed mode = 2048KHz with sample rate 16k. • LE920 supports only the first parameter <**clock**> Normal mode (factory default) = 2048KHz with sample rate 8k. High speed mode = 4096KHz with sample rate 16k. • Another parameters (<**decoder pad**>,<**decoder format**>,<**encoder pad**>,<**encoder format**>)have no effect and are included only for backward compatibility.
AT#DVICFG=?	Test command returns the supported range of values of parameter <**clock**>, <**decoder pad**>,<**decoder format**>,<**encoder pad**>,<**encoder format**>.

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The AT#DVI command enables/disables the DVI interface.
Its syntax is the following:

AT#DVI=<mode> [,<dviport>, <clockmode>]	Set command enables/disables the Digital Voiceband Interface. **Parameters:** **<mode>** - enables/disables the DVI. 0 – DVI disabled; (factory default) 1 – DVI enabled; **<dviport>** 2 - DVI port 2 (factory default) **<clockmode>** 0 - DVI slave (mode not supported) 1 - DVI master (factory default) **Note:** #DVI parameters are saved in the extended profile LE910/LE920 support "DVI master" mode only. The <dviport> and <clockmode> parameters have no effect and are included only for backward compatibility with the Telit On Active/MT/MO Voice Call return Error.
AT#DVI?	Read command reports last setting, in the format: #DVI: <mode>,<dviport>,<clockmode>
AT#DVI=?	Test command reports the range of supported values for parameters <mode>,<dviport> and <clockmode>
Example	AT#DVI=1,2,1 OK DVI activated for audio. DVI is configured as master providing on DVI Port #2

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The LE910 modules have the following possible configurations:

Normal mode (factory default)

- Master Mode
- 8KHz
- 16 bits
- 128KHz clock

High Speed mode

- Master Mode
- 16KHz
- 16 bits
- 2.048MHz clock

The LE920 modules have the following possible configurations:

Normal mode (factory default)

- Master Mode
- 8KHz
- 16 bits
- 2.048MHz clock

High Speed mode

- Master Mode
- 16KHz
- 16 bits
- 4.096MHz clock

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2.3. Timing Characteristics

Parameter	Description	Min	Typical	Max	Units
t(sync)	PCM_SYNC cycle time	-	125	-	us
t(syncha)	PCM_SYNC asserted time	-	488	-	ns
t(syncd)	PCM_SYNC de-asserted time	-	124.5	-	us
t(clk)	PCM_CLOCK cycle time	-	488	-	ns
t(clkh)	PCM_CLOCK high time	-	244	-	ns
t(clkl)	PCM_CLOCK low time	-	244	-	ns
t(sync_offset)	PCM_SYNC offset time to PCM_CLOCK falling	-	122	-	ns
t(sudin)	PCM_RX setup time to PCM_CLOCK falling	60	-	-	ns
t(hdin)	PCM_RX hold time after PCM_CLOCK falling	60	-	-	ns
t(pdout)	Delay from PCM_CLOCK rising to PCM_TX valid	-	-	60	ns
t(zdout)	Delay from PCM_CLOCK falling to PCM_TX HIGH-Z	-	-	60	ns

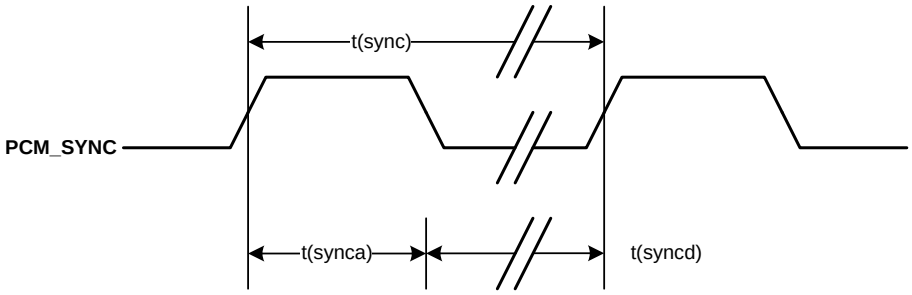

Figure 5. Primary PCM_SYNC timing (Short sync, 2048kHz clock)

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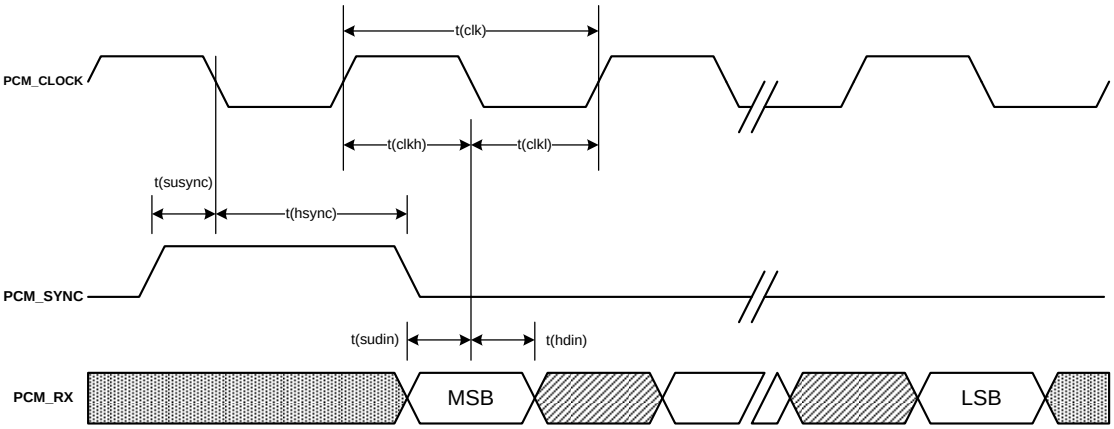

Figure 6. External codec to LE910 timing

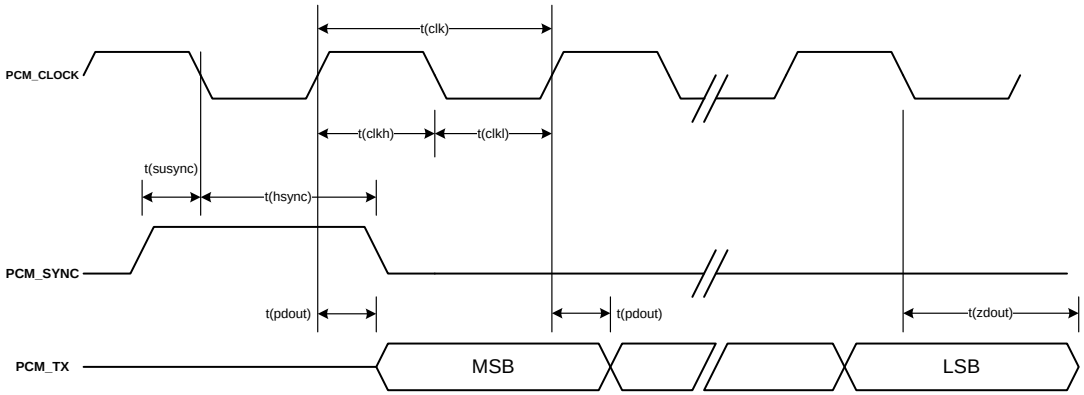

Figure 7. LE910 to External codec timing

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3. DVI Setting

The next chapters show how to configure an external codec connected to the Module.
All the following setting examples are performed using the hardware configuration shown in

fig. 2.

I²C bus is used to configure the MAX9867 Codec[1] [2].
The DVI bus provides the voice connection between the two devices.

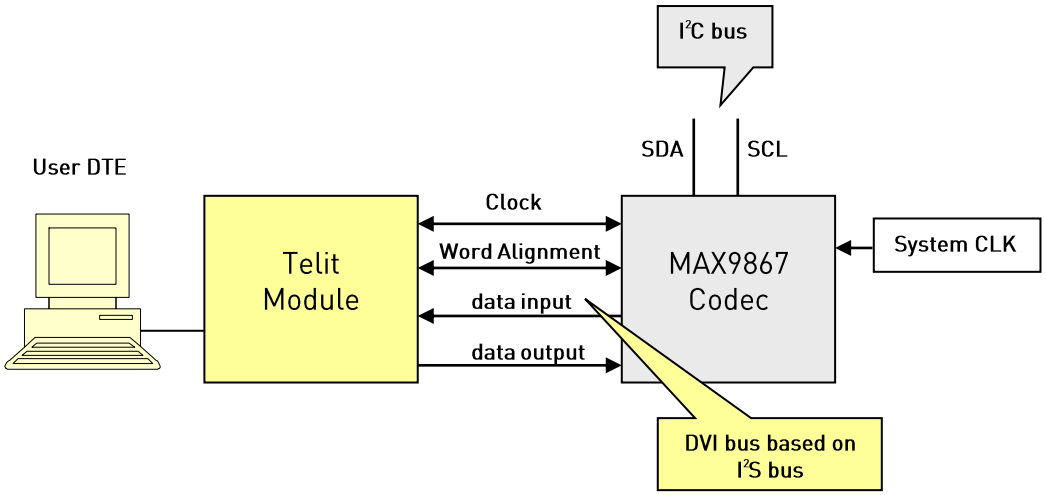

fig. 2: Telit Module/Codec Connections

NOTE: The CODEC Example is applicable only to the High Speed mode

- Master Mode
- 16KHz
- 16 bits
- 2.048MHz clock

[1] The following examples use the MAX9867 Codec, see chapter 4.2 for a schematic reference design. In general, the user can use any codec compliant with the technical requirements of the Telit's modules.

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The module has the role of master. In this case, the WAO and CLK signals are generated by the module. The WAO signal defines the frame of the audio channel.

The following part is showing the commands necessary to set the DVI and the codec

Configure the DVI

DVI bus

AT#DVICFG=1,1,2,1,2
OK

1	High Speed Mode
1	decoder pad enabled
2	decoder format Linear
1	encoder pad enabled
2	encoder format Linear

Set the Module in Master Mode

DVI bus

AT#DVI=1,2,1
OK

1	enable DVI interface
2	use DVI port 2 (mandatory)
1	set the module as Master (factory setting)

Configure the codec in Slave , PCM, Burst (I^2S) Mode

I^2C bus

AT#I2CWR=X,Y,30,4,19
>00109000040000003000000000B0B3414C00000

OK

X	GPIO number used as SDA, refer to [3]
Y	GPIO number used as SCL, refer to [3]
30	Device address on I^2C, refer to [2]
4	Register address from which start the writing, refer to [2]
19	number of bytes to write

>00101000…..refer to [2]

AT#I2CWR=X,Y,30,17,1
>8A
OK

X	GPIO number used as SDA, refer to [3]
Y	GPIO number used as SCL, refer to [3]
30	Device address on I^2C, refer to [2]
17	Register address where write data, refer to [2]
1	number of bytes to write

>8A, refer to [2]

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The CODEC configuration is described in the following table (refer to the MAX9867 datasheet for the details):

Register address	Register Name	Value (Hex)	Value (Bin)	Description
0x04	Interrupt Enable	0	0	Disabled
0x05	System Clock	10	10000	MCLK is between 10MHz and 20MHz (12.288MHz in our example); Frequency: Normal mode The frequency of LRCLK is set by the NI divider bits. Due to the fact the COD is Slave, it expects an LRCLK as specified by the divide ratio
0x06	Audio Clock High	20		NI=0x2000 --> 16KHz
0x07	Audio Clock Low	0	0	
0x08	Interface mode 1a	4	100	MAS=0 : The MAX9867 operates in slave mode with LRCLK and BCLK configured as inputs. WCI ignored because TDM=1 BCI=0 : SDIN is latched into the part on the rising edge of BCLK. SDOUT transitions after the rising edge of BCLK as determined by SDODLY*. DLY ignored because TDM=1 HIZOFF=0 : SDOUT goes to a high-impedance state after all data bits have been transferred out of the MAX9867, allowing SDOUT to be shared by other devices. TDM=1 : LRCLK is a framing pulse that transitions polarity to indicate the start of a frame of audio data consisting of multiple channels. When operating in TDM mode, the left channel is output immediately following the frame sync pulse. If rightchannel data is being transmitted, the 2nd channel of data immediately follows the 1st channel data.
0x09	Interface mode 1b	0	0	LVOLFIX=0 : DMONO=0 : Stereo data input on SDIN is processed separately. BSEL=0 : No effect becasue in Slave Mode
0x0A	Codec Filters	33	110011	MODE=0 : 0 = IIR Voice Filters AVFLT = 0x3 : Filter Eliptical, Sample Rate 8KHz, HighPass Corner Freq 256Hz, 217Hz Notch active. DVFLT= 0x3 : Filter Eliptical, Sample Rate 8KHz, HighPass Corner Freq 256Hz, 217Hz Notch Active.
0x0B	DAC Gain/Sidetone	0	0	DSTS=0 : 00 = No sidetone is selected. DVST=0 : Disabled
0x0C	DAC Level	0	0	DACM=0 : NO Mute DACG=0 : 0dB DACA=0 : 0dB Gain
0x0D	ADC Level	33	110011	AVL=0x3 : 0dB Gain AVR=0x3 : 0dB Gain
0x0E	Left Line Input Level	0C	1100	LILM=0 : Line input is connected to the headphone amplifiers. LIRM=0 : Line input is connected to the headphone amplifiers.
0x0F	Right Line Input Level	0C	1100	LIGL = 0xC : 0dB Gain LIGR = 0xC : 0dB Gain

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0x10	Left Volume Control	9	1001	VOLLM=0 : Audio playback is unmuted. VOLL=0x9 : 0dB Gain
0x11	Rigth Volume Control	9	1001	VOLRM=0 : Audio playback is unmuted. VOLR= 0x9 : 0dB Gain
0x12	Left Mic Gain	24	100100	PALEN=0x01 : PreAmplifier Gain=0dB PGAML=0x4 : Gain =+16dB
0x13	Rigth Mic Gain	24	100100	PALEN=0x01 : PreAmplifier Gain=0dB PGAML=0x4 : Gain =+16dB
0x14	ADC Input	40	1000000	MXNL= 01 = Left analog microphone MXNR= 00 = No Input selected AUXCAP=0 : Update AUX with the voltage at JACKSNS/AUX. AUXGAIN=0 : Normal operation AUXCAL=0 : Normal operation AUXEN=0 : Use JACKSNS/AUX for jack detection.
0x15	Microphone	0	0	MICCLK=0 : PCLK/8 DIGMICL=0 and DIGMICR=0 : Left ADC input= ADC input mixer, Right ADC Input=ADC input mixer.
0x16	Mode	60	1100000	DSLEW=0 : Digital volume changes are slewed over 10ms. VSEN*=1 : Volume changes occur in one step. ZDEN*=1 : Line-input volume changes occur immediately. JDETEN=0 : Enables pullups on LOUTP and JACKSNS/AUX to detect jack insertion. LSNS and JKSNS are valid. LOUTP detection is only valid in differential and capacitorless output modes. HPMODE=0 : Stereo differential (clickless)
0x17	System Shutdown	8A	10001010	SHDN*=1 : Places the device in low-power shutdown mode. LNLEN=0 : Left-Line Input disabled LNREN=0 : Rigth-Line Input disabled DALEN=1 : Enables the left DAC and automatically enables the left and right headphone amplifiers. DAREN=0 : Right DAC disabled ADLEN=1 : Left ADC Enabled ADREN=0 : Right ADC disabled

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4. Annex

4.1. I²S Overview

This chapter provides a short description of the standard I2S bus. This standard suitably modified is used by the DVI interface implemented on the Telit's modules.

The standard I2S is an electrical serial bus designed for connecting digital audio devices. This popular serial bus has been developed by Philips® in 1986 as a 3-wire bus for interfacing to audio chips such as codecs. It is a simple data interface, without any form of address or device selection.

Refer to fig. 3: the I2S design handles audio data separately from clock signals. On an I2S bus, there is only one bus master and one transmitter.

In high-quality audio applications involving a Codec, the Codec is typically the master so that it has precise control over the I2S bus clock.

An I2S bus design consists of the following serial bus lines:

- SD: Serial Data
- WS: Word Select
- Serial Clock: SCK

The I2S bus carries two channels (left and right) 8 bit long, which are typically used to carry stereo audio data streams. The data alternates between left and right channels, as controlled by the word select signal driven by the bus master.

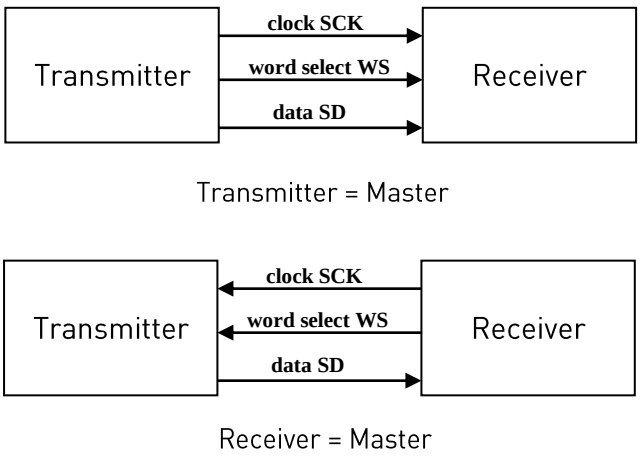

fig. 3: I²S bus configurations

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4.2. Schematic

A schematic example of an interface between the Telit's modules and the MAX9867 CODEC could be the following:

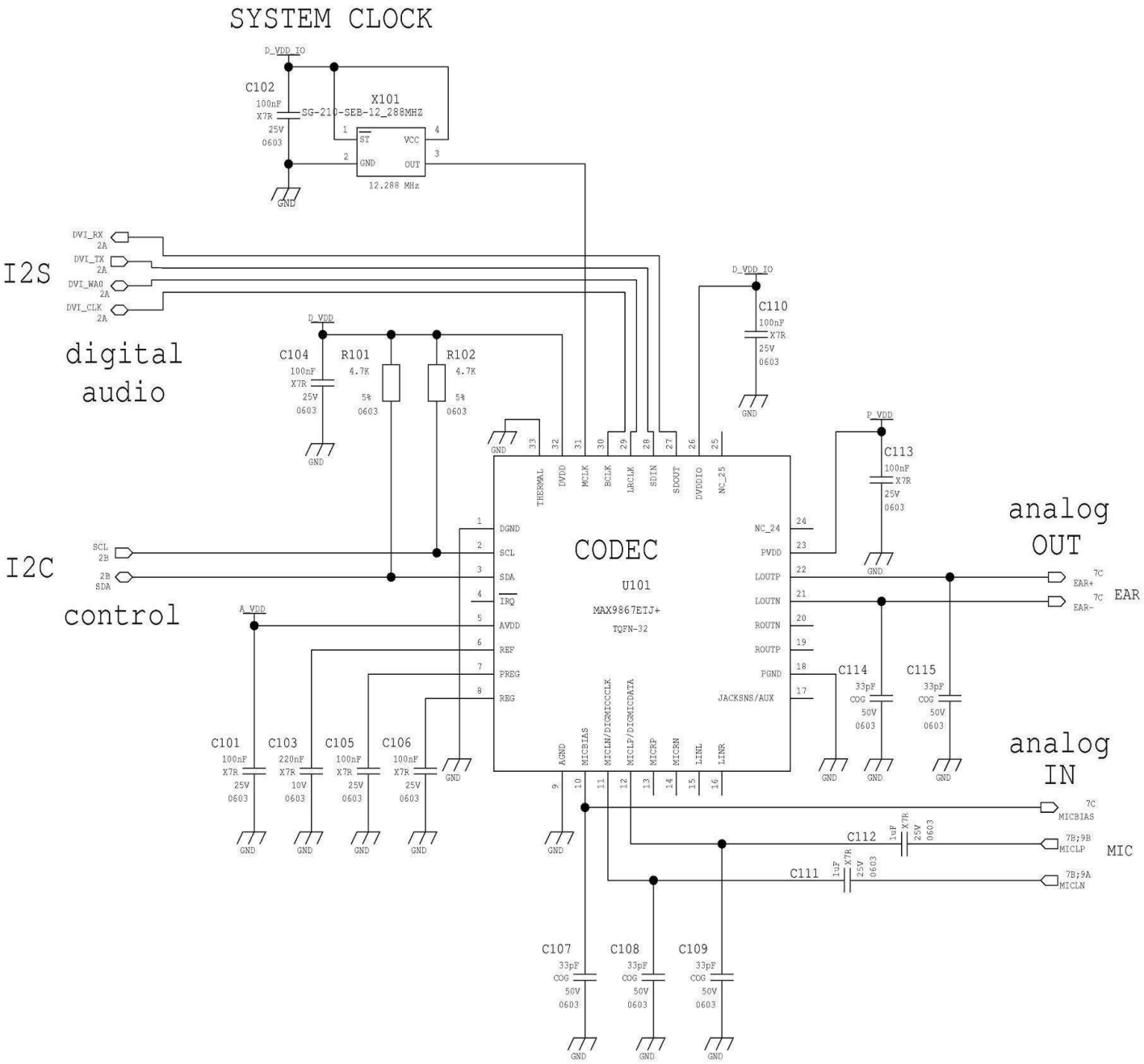

fig. 4: Schematic for Reference Design

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