HE910/UE910 USB HSIC
Application Note

80000NT10071A - Rev. 1 – 2013-12-20

Making machines talk.

Applicability Table

PRODUCT
HE910 (*)
HE910-GA
HE910-D
HE910-EUR
HE910-EUD
HE910-EUG
HE910-NAR
HE910-NAD
HE910-NAG
UE910-EUR
UE910-EUD
UE910-NAR
UE910-NAD

(*) HE910 is the “type name” of the products marketed as HE910-G & HE910-DG

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Contents

1. Introduction 6
1.1. Scope 6
1.2. Audience 6
1.3. Contact Information, Support 6
1.4. Document Organization 7
1.5. Text Conventions 8
1.6. Related Documents 8
1.7. Document History 9
1.8. Abbreviation and Achronyms 9

2. Overview 10
2.1. USB HSIC description 10

3. USB HSIC Hardware Interface 11
3.1. USB HSIC Hardware Signals and Protocol 11
3.1.1. Logic Levels Specifications 13
3.1.2. Additional Electrical Specifications 14
3.1.3. STROBE and DATA HSIC signals 15
3.1.4. USB HSIC power management 16
3.1.5. Additional HSIC signals 17
3.2. USB HSIC PCB Design Considerations 17

4. USB HSIC Interface Initialization 18
4.1. Enabling the USB HSIC 18
4.2. HSIC Initialization and Enumeration 18

5. SAFETY RECOMMENDATIONS 20

1. Introduction

1.1. Scope

The aim of this document is the description of some hardware solutions useful for developing an application that interfaces the HE910/UE910 through the USB HSIC Port.

1.2. Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our HE910/UE910 modules.

1.3. Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit's Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.

1.4. Document Organization

This document contains the following chapters.

Chapter 1: "*Introduction*" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "*USB HSIC Overview*" provides an overview of the document.

Chapter 3: "*Hardware Interface*" provides a detailed description of the HSIC signals.

Chapter 4: "USB HSIC Initialization"

Chapter 5 "SAFETY RECOMMENDATIONS".

1.5. Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

1.6. Related Documents

- AT Commands Reference Guide 80378ST10091A
- HE910 HW User Guide 1vv0300925
- UE910 HW User Guide 1vv0301012
- HE910/UE910 Ports Arrangements User Guide 1vv0300971
- High Speed Inter Chip USB Interface Specification v 1.0 (USB.ORG)
- USB Engineering Change Notice May 21th, 2012

1.7. Document History

Revision	Date	Changes
ISSUE#0	2012-06-11	First release
ISSUE#1	2013-12-20	Overall review of the document; added the UE910 products

1.8. Abbreviation and Achronyms

DTE	Data Terminal Equipment
HSIC	High Speed Inter Chip Interface
AP	Application Processor
CP	Communication Processor
PCB	Printed Circuit Board
USB	Universal Serial Bus
NRZI	Non Return to Zero Inverted Encoding
HSPA	High Speed Packet Access
LPM	Link Power Management
PHY	Physical Layer

2. Overview

This document cannot embrace the whole hardware solutions and products that may be designed. The suggested hardware configurations shall not be considered mandatory; instead the information given shall be used as a guide or a starting point for properly developing your product with the Telit modules.
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2.1. USB HSIC description

The USB HSIC (High Speed Inter Processor) Interface allows supporting the inter-processor communication between an application processor (AP) – the host, and the modem processor (CP) – the Module.
The USB HSIC is a variant of USB 2.0 that eliminates the conventional analog transceivers found in normal USB. The HSIC hardware interface uses less power and occupies less PCB area compared to traditional USB 2.0. USB HSIC is a half-duplex connection offering a 480 Mbit/s data rate, making USB HSIC suitable for HSPA+ and LTE, where data throughputs are about 40Mbps and 150Mbps, respectively. An additional advantage of USB HSIC is to re-use the widely developed standard USB driver architecture on both AP and CP, for example on Linux (Android) platforms.
This application note contains details on the USB HSIC hardware interface along with information pertinent to the software implementation on USB HSIC.
In a typical configuration, the Module acts as a wireless modem while the AP runs all the applications and multimedia features.
The command flow is implemented using a logical channel multiplexer and AT commands. The use of the logical channels allows low latency communication (Data) to be performed independently of the longer latency communications (control).

3. USB HSIC Hardware Interface

As discussed, USB HSIC is a variant of USB 2.0 specifically designed for chip-to-chip communications. It eliminates the conventional Analog transceivers found in normal USB. HSIC uses two signals at 1.2 V and has a throughput of 480 Mbit/s.
The USB controller is compliant to the USB 2.0 Specification, the HSIC electrical specification, and the Link Power Management (LPM) Addendum.

The USB HSIC on the Module supports the following features:

- Device mode
- High Speed (480 Mbit/s)
- Link Power Management (LPM)

3.1. USB HSIC Hardware Signals and Protocol

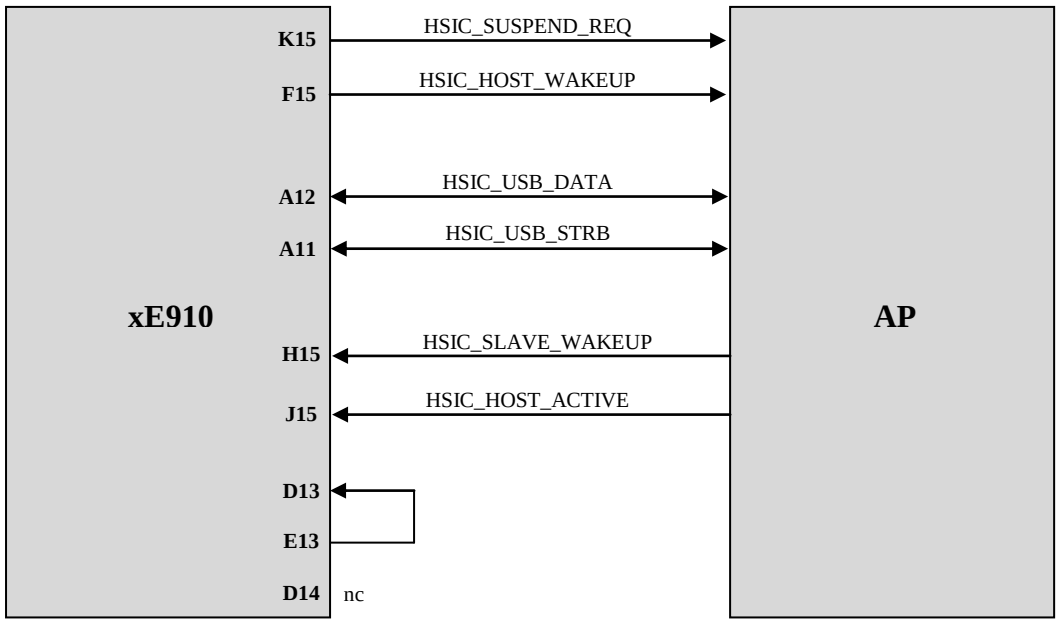
The USB HSIC consists of a 2-wire serial interface (HSIC_USB_DATA & HSIC_USB_STRB) that operates at 1.2 V.
Both data and strobe are bi-directional, NRZI encoded.
Even though USB HSIC as itself is enough to communicate between the AP and CP, two additional signals are required.
The main purpose of these two lines is to signal a specific event from the AP to the CP or from the CP to the AP. This will be used during the system boot and for power optimization.

For further power reduction, the USB HSIC supports the link power management (LPM) feature according to the USB2.0 standard.
The LPM defines power management states and mechanisms to affect state changes that are used by the AP and CP to efficiently manage bus and system power.
To take advantage of the LPM feature, an additional two signals are needed. The signals are needed to support power management state transitions.
The two additional signals support the SUSPEND and HOST_ACTIVE functions.

The Module provides the USB HSIC signals on the following pads:

#	Signal	Direction	Function	Type	COMMENT
A12	HSIC_USB_DATA	AP↔CP	USB HSIC data signal	CMOS 1.2V	
A11	HSIC_USB_STRB	AP↔CP	USB HSIC strobe signal	CMOS 1.2V	
H15	HSIC_SLAVE_WAKEUP	AP→CP	Used by AP to wakeup CP	CMOS 1.8V	Shared with SPI_MRDY
F15	HSIC_HOST_WAKEUP	AP←CP	Used by CP to wakeup AP	CMOS 1.8V	Shared with SPI CLK
K15	HSIC_SUSPEND_REQUEST	AP←CP	Used by CP in ON state to indicate that USB link can be switch to SUSPEND because CP has no data to transfer.	CMOS 1.8V	Shared with GPIO08
J15	HSIC_HOST_ACTIVE	AP→CP	Inactive: USB on AP is switched off. Active: USB on AP is switched on. Used to synchronize enumeration.	CMOS 1.8V	Shared with SPI_SRDY
D13	VDD_IO1	I	IO1 SUPPLY Input		To be connected with E13
E13	VIO1_1V8	O	VIO1 Supply output (1.8V)		To be connected with D13

A diagram of the USB HSIC hardware solution including the additional signals for power management is shown in this picture:



3.1.1. Logic Levels Specifications

The following table shows the logic level specifications used in the Module's interface circuits:

Absolute Maximum Ratings - Not Functional

Parameter	Min	Max
Input level on any digital pin (CMOS 1.8) with respect to ground	-0.3V	2.1V
Input level on any digital pin (CMOS 1.2) with respect to ground	-0.3V	1.4V

Operating Range - Interface levels (1.8V CMOS)

Level	Min	Max
Input high level	1.5V	1.9V
Input low level	0V	0.35V
Output high level	1.6V	1.9V
Output low level	0V	0.2V

Operating Range - Interface levels (1.2V CMOS)

Level	Min	Max
Input high level	0.9V	1.3V
Input low level	0V	0.3V
Output high level	1V	1.3V
Output low level	0V	0.1V

Current characteristics

Level	Max
Output Current	1mA
Input Current	1uA

3.1.2. Additional Electrical Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
I/O pad drive strength	O_D	40		60	Ω	1
Pull-up/pull-down bus keeper resistor	R_K	20		50	KΩ	5
Alternate pull-up resistor	R_{PU-ALT}	2		5	KΩ	5
Alternate pull-down resistor	R_{PD-ALT}	20		50	KΩ	5
I/O input impedance	Z_i	240			KΩ	
Buffer load	BL	1		5	pF	
Characteristic trace impedance	T_I	45	50	55	Ω	4
Circuit board trace length	T_L	2		10	Cm	4
Circuit board trace propagation skew	T_S			15	ps	3, 4
STROBE frequency	F_{STROBE}	239.88	240	240.12	MHz	2
Slew rate (rise & fall) STROBE & DATA	T_{slew}	0.7		2	V/ns	2, 6, 7
Receiver DATA Setup time (with respect to STROBE)	T_s	365			ps	2, 8
Transmitter uncertainty	T_T	365			ps	2, 8
Receiver DATA Hold time (with respect to STROBE)	T_h	300			ps	2, 8

Notes

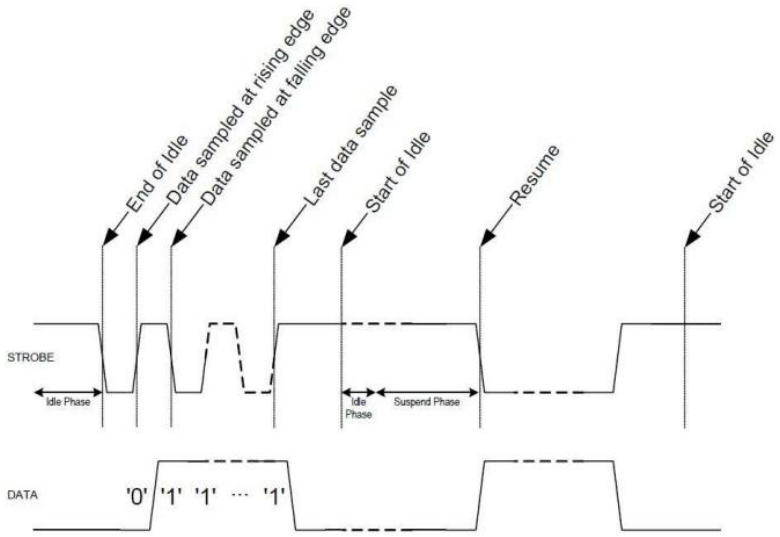
1: Controlled output impedance driver
2: Jitter and duty cycle are not separately specified parameters, they're incorporated into the above table values
3: Max propagation delay skew in STROBE and DATA with respect to each other. The trace delay should be matched between STROBE and DATA to ensure that signal timing is within specification limits at the receiver
4: Informative only
5: The bus keeper values implemented depend on power up sequence assumptions
6: Measured at transmitter with capacitive test load of 3 pF
7: Averaged form 30% - 70% points
8: Measured at the 50% point

For more detailed information please refer to:

- High-Speed Inter-Chip USB Electrical Specification Ver. 1.0 – September 23rd, 2007
- USB Engineering Change Notice – May 21th, 2012

3.1.3. STROBE and DATA HSIC signals

As depicted below, HSIC_USB_STRB is a Clock signal. HSIC_USB_DATA is a Data line, sampled on Strobe signal rising and falling edge:



STROBE and DATA signals states are also used to indicate the USB host and device states:

Status	Strobe	Data	Description
IDLE	Hi	Lo	1 or more Strobe-periods
CONNECT	Lo	Hi	2 Strobe-periods
RESUME	Lo	Hi	For time periods per USB 2.0 SPEC
SUSPEND	Hi	Lo	Per USB 2.0 SPEC
RESET	Lo	Lo	Per USB 2.0 SPEC

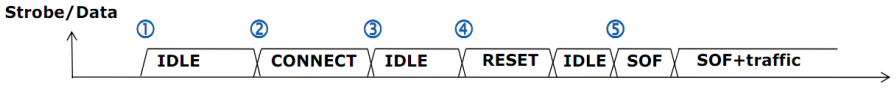
NOTE:

Correct Data and Strobe scopes are obtained by:

- Using very low capacitance, High Impedance probes;
- Considering lines reflections, causing voltage levels differences on different line probing points;
- Using a 20Gs or more bandwidth scope, due to fact signals toggle at 240MHz.

The connect and enumeration sequence is performed in the following way:

1) Host and Device power-up, bus is kept in IDLE by host bus keepers;
2) Device detects IDLE state and drives CONNECT;
3) Device stops driving CONNECT;
4) Host issues RESET;
5) Host starts sending SOF and traffic as per normal USB enumeration.



3.1.4. USB HSIC power management

The available states are the following:

- USB Active (L0)
- USB Suspend (L2 PHY On) → as per USB specification
- USB Suspend (L2 PHY Off) → Low power Consumption
- USB Disconnected (L3) → Not defined in USB HSIC specification.

USB State	AP Core	AP PHY	AP Deep Sleep	CP Core	CP PHY	CP Deep Sleep
USB Active (L0)	YES	YES	NO	YES	YES	NO
USB Suspend (L2 PHY On)	YES	YES	YES	NO	YES	YES
USB Suspend (L2 PHY Off)	YES	NO	YES	NO	NO	YES
USB Disconnected (L3)	NO	NO	YES	NO	NO	YES

The following table is showing the allowed link state transitions:

FROM / TO	L0	L2 PHY On	L2 PHY Off	L3
USB Active (L0)	X	AP/CP(*)	AP/CP(*)	X
USB Suspend (L2 PHY On)	AP/CP	X	X	AP
USB Suspend (L2 PHY Off)	AP/CP	X	X	AP
USB Disconnected (L3)	AP/CP	X	X	X

(*) CP requests suspend through SuspendRequest GPIO.
AP does not have to fulfill the request if it has data to transfer.

3.1.5. Additional HSIC signals

Besides STROBE and DATA, 4 additional lines are used as part of the USB HSIC bus. As previously stated, Host Active, Slave Wakeup, Suspend Request and Host Wakeup implement the so called USB Link Power Management.
Their tasks are here described:

Control Line	Description
HSIC_HOST_ACTIVE	**Inactive:** The Host Controller is switched Off. **Active:** The Host Controller is switched On (Used to synchronize enumeration)
HSIC_SLAVE_WAKEUP	Used by AP to wakeup CP when in L2 or L3
HSIC_SUSPEND_REQUEST	Used by CP in L0 to indicate that link can be switched to L2 because CP has no data to transfer.
HSIC_HOST_WAKEUP	Used by CP to resume link from L2 or L3 to L0 when data is available on CP.

3.2. USB HSIC PCB Design Considerations

The HSIC_USB_STRB and HSIC_USB_DATA are high-speed signals and should be routed as 50 ohm impedance traces. The trace length of these signals should be balance to minimize timing skew.
The active level for the AP & CP WAKEUP lines could not be specified because depending on the Application hardware implementation.
HSIC_HOST_WAKEUP and HSIC_SLAVE_WAKEUP lines are mandatory and their state has to always be valid even when AP or CP goes into power saving mode. External pull-up/pull-down should be used for this purpose.
The distance between the modem and the AP must not exceed 10 cm.

4. USB HSIC Interface Initialization

This section of the document describes the flow of activities necessary to startup the HSIC bus.

4.1. Enabling the USB HSIC

The HE910/UE910 modules are not providing the USB HSIC port by default.
The feature has to be enabled using a dedicated AT Command (AT#PORTCFG).
Please refer to the AT Commands and Ports Arrangements user guides for the detailed command description and syntax.

4.2. HSIC Initialization and Enumeration

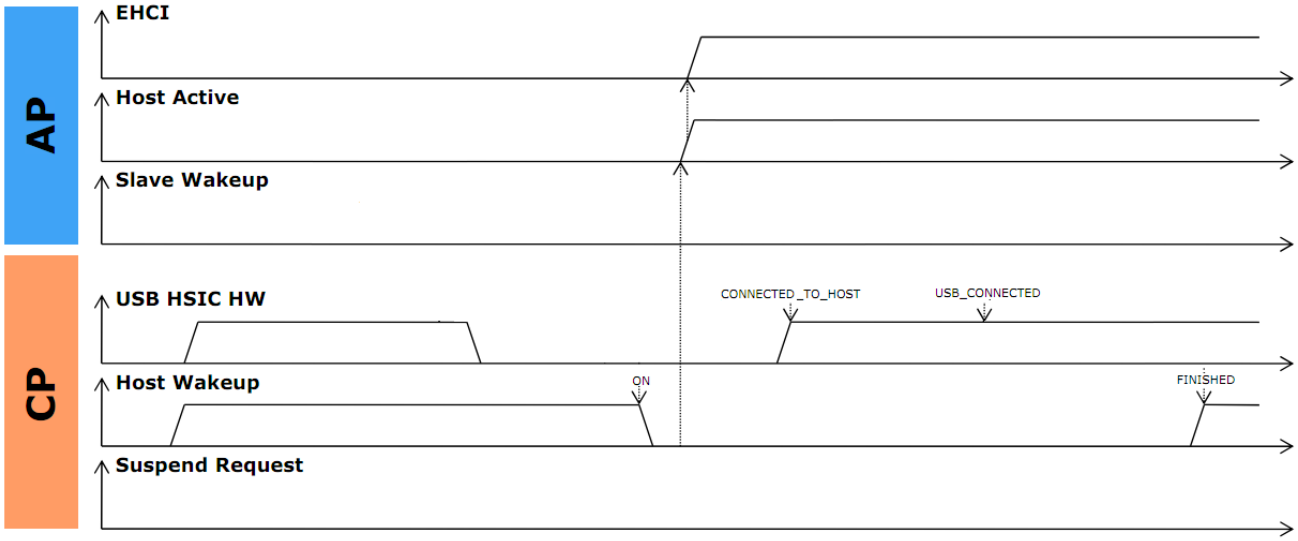
The following diagrams and scopes describe the suggested CP power up and CP/AP control lines statuses for the correct HSIC startup and enumeration:

1) AP Powered up and completed OS boot-up. HSIC EHCI controller is off at this stage.
   AP Drives the HSIC_HOST_ACTIVE line to Low (0V)
2) At any given time, AP powers CP on.
   CP drives the HSIC_HOST_WAKEUP line to High (1.8V) during boot-up phase and starts HSIC Extended Link Power Management (ELPM) Initialization.
3) Upon completion of CP boot-up and ELPM initialization, the CP drives the HSIC_HOST_WAKEUP to low. CP HSIC device is OFF at this stage.

NOTE: The AP can use the HSIC_HOST_WAKEUP falling edge (of step 3) to trigger the transition to step 4.

4) AP turns on the HSIC EHCI controller.
   NOTE: Make sure that EHCI controller is ready (IDLE on the BUS) before continuing to step 5.
5) The AP drives the HSIC_HOST_ACTIVE to High.
6) CP detects as interrupt the HSIC_HOST_ACTIVE set to High. Upon detection, CP turns on the HSIC device controller then CP sets CONNECT bus state.
   AP sends RESET, SOF, GET DESCRIPTOR, etc….
7) Upon successful completion of the enumeration sequence, CP drives the HSIC_HOST_WAKEUP line to high

Now the HSIC controllers and the control signals are synchronized between the AP and CP.
This concludes the handshake sequence for the enumeration.



5. SAFETY RECOMMENDATIONS

NOTE. Read this section carefully to ensure the safe operation.

Be sure the use of this product is allowed in the country and in the environment required. The use of this product may be dangerous and has to be avoided in the following areas:
Where it can interfere with other electronic devices in environments such as hospitals, airports, aircrafts, etc
Where there is risk of explosion such as gasoline stations, oil refineries.
It is responsibility of the user to enforce the country regulation and the specific environment regulation.
Do not disassemble the product; any mark of tampering will compromise the warranty validity.

We recommend following the instructions of the hardware user guides for a correct wiring of the product. The product has to be supplied with a stabilized voltage source and the wiring has to be conforming to the security and fire prevention regulations.

The product has to be handled with care, avoiding any contact with the pins because electrostatic discharges may damage the product itself. Same cautions have to be taken for the SIM, checking carefully the instruction for its use. Do not insert or remove the SIM when the product is in power saving mode.
The system integrator is responsible of the functioning of the final product; therefore, care has to be taken to the external components of the module, as well as of any project or installation issue, because the risk of disturbing the GSM network or external devices or having impact on the security. Should there be any doubt, please refer to the technical documentation and the regulations in force.
Every module has to be equipped with a proper antenna with specific characteristics. The antenna has to be installed with care in order to avoid any interference with other electronic devices and has to guarantee a minimum distance from the body (20 cm). In case of this requirement cannot be satisfied, the system integrator has to assess the final product against the SAR regulation EN 50360.

The European Community provides some Directives for the electronic equipments introduced on the market. All the relevant information are available on the European Community website:
http://europa.eu.int/comm/enterprise/rtte/dir99-5.htm

The text of the Directive 99/05 regarding telecommunication equipments is available, while the applicable Directives (Low Voltage and EMC) are available at:
http://europa.eu.int/comm/enterprise/electr_equipment/index_en.htm