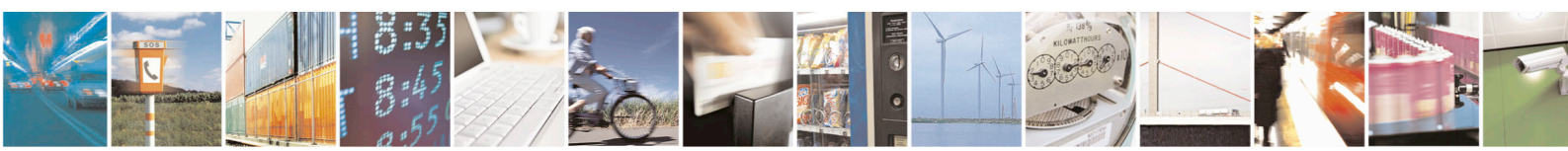
UE/HE910V2_DE/CE910_HE920_CL865
Digital Voice Interface
Application Note

80000NT10101A Rev.1 2015-06-19

Making machines talk.

APPLICABILITY TABLE

PRODUCT
DE910-xxx
HE910-xxx V2
CE910-xxx
UE910-xxx V2
HE920-xxx
CL865-xxx



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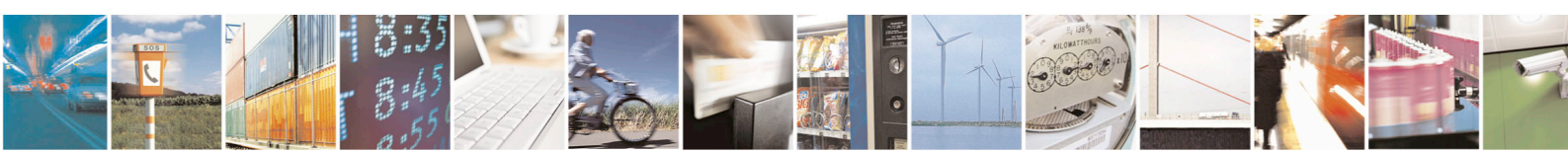
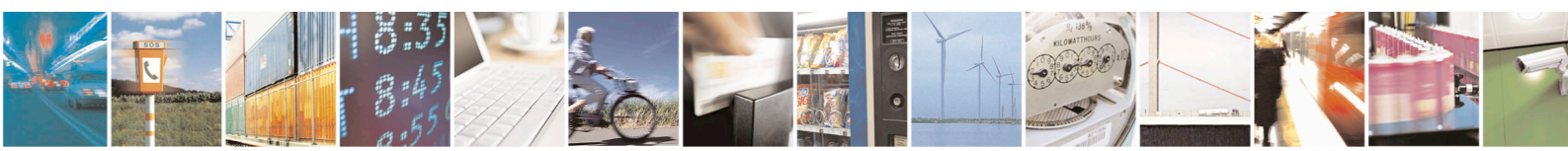


Contents



1 Introduction

1.1 Scope

The aim of this document is the description of some hardware specification useful to develop a product using Telit modules supporting DVI (PCM), as specified in the aforementioned applicability table.

1.2 Audience

This document is intended for Telit customers, who are integrators, about to implement their applications using our UE/HE910V2_DE/CE910_HE920_CL865 modules.

1.3 Contact Information, Support

For general contact, technical support, to report documentation errors and to order manuals, contact Telit's Technical Support Center (TTSC) at:

TS-EMEA@telit.com
TS-NORTHAMERICA@telit.com
TS-LATINAMERICA@telit.com
TS-APAC@telit.com

Alternatively, use:

http://www.telit.com/en/products/technical-support-center/contact.php

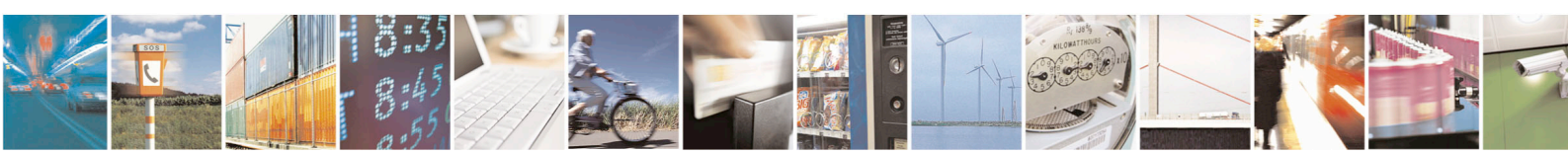
For detailed information about where you can buy the Telit modules or for recommendations on accessories and components visit:

http://www.telit.com

To register for product news and announcements or for product questions contact Telit's Technical Support Center (TTSC).

Our aim is to make this guide as helpful as possible. Keep us informed of your comments and suggestions for improvements.

Telit appreciates feedback from the users of our information.



1.4 Document Organization

This document contains the following chapters:

Chapter 1: "Introduction" provides a scope for this document, target audience, contact and support information, and text conventions.

Chapter 2: "Overview" provides an overview of the document.

Chapter 3: "UE/HE910V2_DE/CE910_HE920_CL865 DVI" describes the DVI port as far as the UE/HE910V2_DE/CE910_HE920_CL865 modules are concerned

Chapter 4: "Protocol description"

Chapter 5: "Parameters and timing characteristics"

Chapter 6: "Custom AT commands"

Chapter 7: "External codec" provides an example of interfacing with an external audio codec.

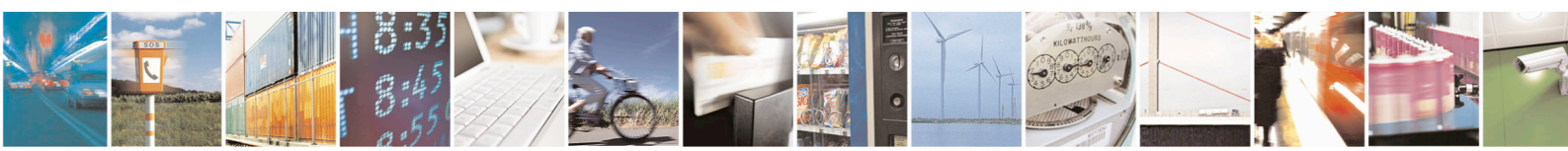
1.5 Text Conventions

Danger – This information MUST be followed or catastrophic equipment failure or bodily injury may occur.

Caution or Warning – Alerts the user to important points about integrating the module, if these points are not followed, the module and end user equipment may fail or malfunction.

Tip or Information – Provides advice and suggestions that may be useful when integrating the module.

All dates are in ISO 8601 format, i.e. YYYY-MM-DD.

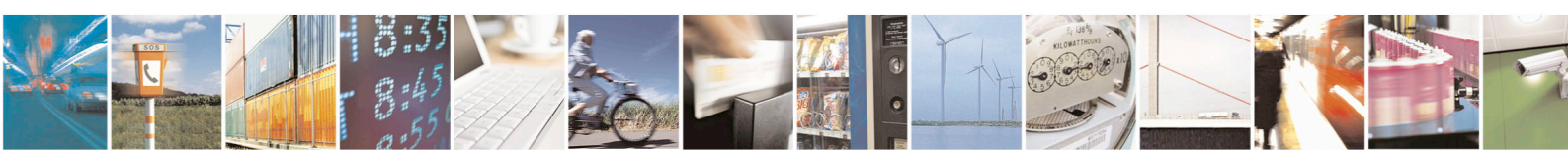


1.6 Related Documents

- Software User guide
- Hardware User Guide
- Product description
- AT Commands Reference Guide

1.7 Document History

Revision	Date	Changes
0	2013-06-25	First release
1	2015-06-19	Fixed figure 3 Deleted figure 4 Added CL865 Changed External Codec to MAX9867



2 Overview

The Telit Modules support the ***Digital Voice Interface*** (from here onwards ***DVI***), which can be used to transfer digital audio data *to* and *from* the module itself.

The ***DVI*** uses the *PCM interface* as part of the audio front end; it easily allows for an external codec to be used instead of the internal codec.

As an example, through the ***DVI*** you could connect a Telit Module to a Bluetooth device.

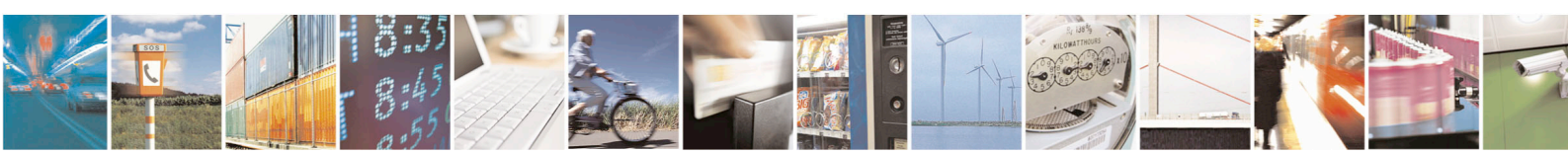
2.1 Hint on PCM

Although analog communication is ideal for human communication, analog transmission is neither robust nor efficient at recovering from line noise.
As example in the early telephony network, when analog transmission was passed through amplifiers to boost the signal, not only was the voice boosted but the line noise was amplified, as well. This line noise resulted in an often-unusable connection.
It is much easier for digital samples, which are comprised of 1 and 0 bits, in order to be separated from line noise. Therefore, when analog signals are regenerated as digital samples, a clean sound is maintained.
PCM converts analog sounds into digital form by sampling the analog sounds 8000 times per second and converting each sample into a numeric code. If you sample an analog signal at twice the rate of the highest frequency of interest, you can accurately reconstruct that signal back into its analog form (Nyquist theorem). Because most speech content is below 4000Hz, a sampling rate of 8000 times per second (8KHz that means 125 µSec between samples) is required.

2.2 General information

The Telit Modules can have one ***DVI*** port.

Please refer to the User Guide of the module that you are using to know the number of the available ***DVI*** port.



3 UE/HE910V2_DE/CE910_HE920_CL865 DVI

The UE/HE910V2_DE/CE910_HE920_CL865 have only one ***DVI*** port (or *Auxiliary Codec Port*), the hardware supports for continual transmission and reception of PCM Data. It has two different modes:

- Standard Operating Mode, actually used
- Standalone Operating Mode, actually not allowed

The activation of the ***DVI function*** does the internal codec automatically disabled, and the user has to interface an external codec (the "*AUXILIARY PCM device*") in order to use it.

Even if the ***Auxiliary Codec Port*** is physically one, you can set it via software in two configuration modes, each one with its own clock frequency, clock format, frame synchronism and clock mode.

The gains (*volumes*) for DOWNLIK and UPLINK paths can be set:

- by the dedicated AT commands
- tuning the gain of the external codec amplifiers (refer to external codec manual)

3.1 Configuration mode

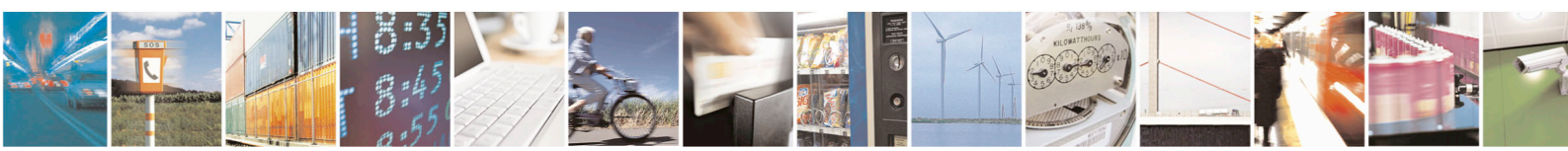
The configuration modes are ***Auxiliary (Normal mode)*** and ***Primary (Highspeed mode).*** The choice depends from the needs of the customer, but always keeping in mind that only *one mode at time* is allowed.

- **Auxiliary** *Configuration Mode* is the *default mode* running at 128 KHz with standard *Long Frame Sync* timing. It supports: *16-bit linear or 8-bit A-Law* or *µ-Law with padding*.

- ***Primary*** *Configuration Mode* is the *other mode* running at 2.048 MHz with *Short Frame Sync* timing. It supports: *16-bit linear* or *8-bit A-Law* or *µ-Law with padding*.

They both use the same hardware path at 8 KHz sample-rate, in burst mode and mono voice data.

A-Law is the PCM variant in Europe, while *µ-Law* is the PCM variant in America.



3.2 Clock Mode

Being a bidirectional interface, you can choose the "direction" of clock for receive and transmit codec PCM data.

The *clock Mode (or in other words the module)* can be:
:

- ***Master*** if UE/HE910V2_DE/CE910_HE920_CL865 are the clock signal source; the ***PCM_CLK*** pin becomes an output and its direction is from UE/HE910V2_DE/CE910_HE920_CL865 to external codec.

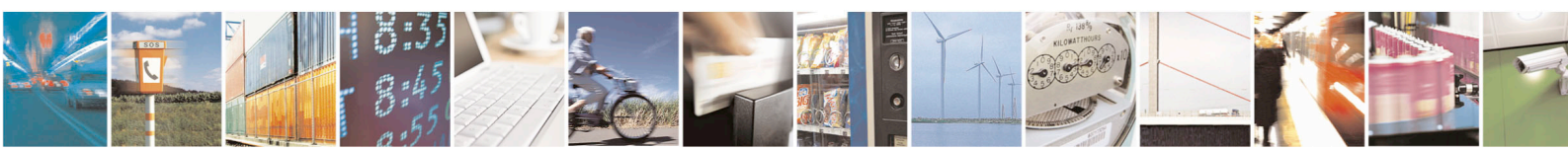
- ***Slave*** if the external "*AUXILIARY PCM device*" is the signal clock source; the ***PCM_CLK*** pin becomes an input and its direction is from external codec to UE/HE910V2_DE/CE910_HE920_CL865.

WARNING:

Slave mode* is not allowed in the "*AUXILIARY Configuration Mode (128K with standard Long sync frame).

3.3 Summary

- the *Digital Voice Interface* allows the use of an external codec .It is Software , and can be the "*AUXILIARY PCM Interface*" (*the default interface*) working at 128KHz clock , or the "*PRIMARY PCM Interface*" (*the other interface*) working at 2.048MHz ;
- the "*AUXILIARY CODEC PORT*" operates at 128KHz when the "*AUXILIARY PCM Interface*" is active
- the "*AUXILIARY CODEC PORT*" operates at 2.048MHz when the "*PRIMARY PCM Interface*" is active
- the "*AUXILIARY CONFIGURATION Mode*" sets the clock frequency/sync type to 128KHz/ long sync
- the "*PRIMARY CONFIGURATION Mode*" sets the clock frequency/sync type to 2.048MHz/ short sync
- the "*MASTER Clock Mode*" sets UE/HE910V2_DE/CE910_HE920_CL865 as clock source
- the "*SLAVE Clock Mode*" sets the external "*AUXILIARY PCM device*" as clock source



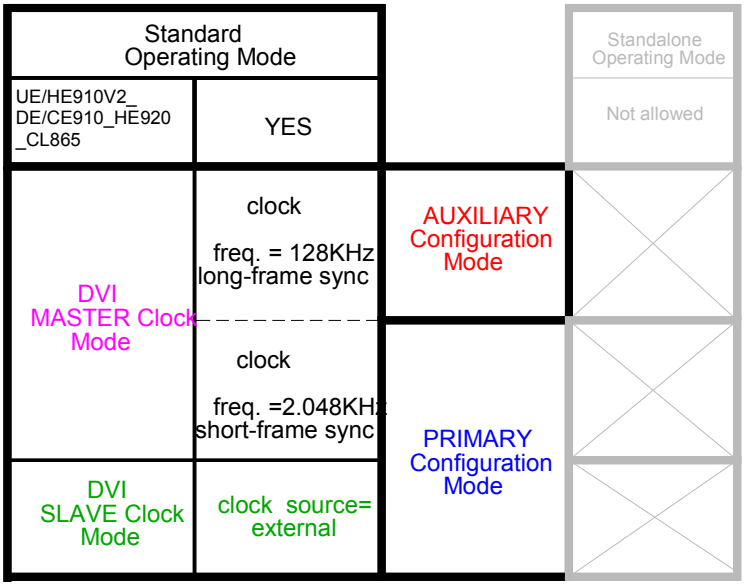


Table 3.1 Settings Map of the Digital Voice Interface

3.4 DVI port pinout

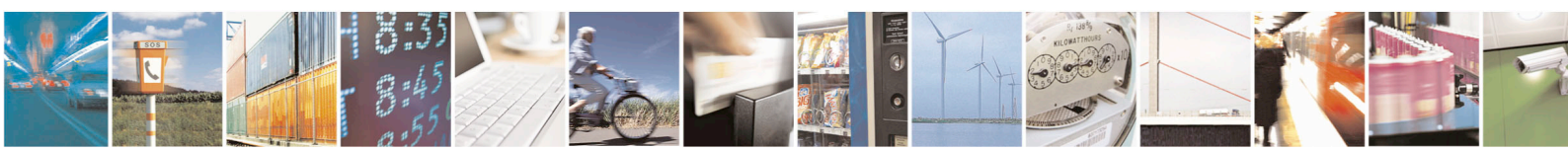
The ***DVI port is*** accessible on four pins on UE/HE910V2_DE/CE910_HE920_CL865. The port itself is mapped on two logical ports, *Auxiliary port* and *Primary port*, depending on the functionality set via AT command.
For the timing diagram of the two different refer to Protocol Description in chapter 3.

According to the applied *Configuration Mode*, you will have on the pins of the UE/HE910V2_DE/CE910_HE920_CL865 PAD signals with different logical names.

The table 2 summarizes the signal and correspondent pin, while the figure 2 is the block diagram of the routing of the same signals.

PAD or Connector PINOUT	Function	Primary PCM Interface	Auxiliary PCM Interface
name		Logical name	
DVI_CLK	Clock in/out	PCM_CLK	AUX_PCM_CLK
DVI_RX	Data in	PCM_DIN	AUX_PCM_DIN
DVI_TX	Data out	PCM_DOUT	AUX_PCM_DOUT
DVI_WA0	Synchronism	PCM_SYNC	AUX_PCM_SYNC

Table 3.2 Signal name Map



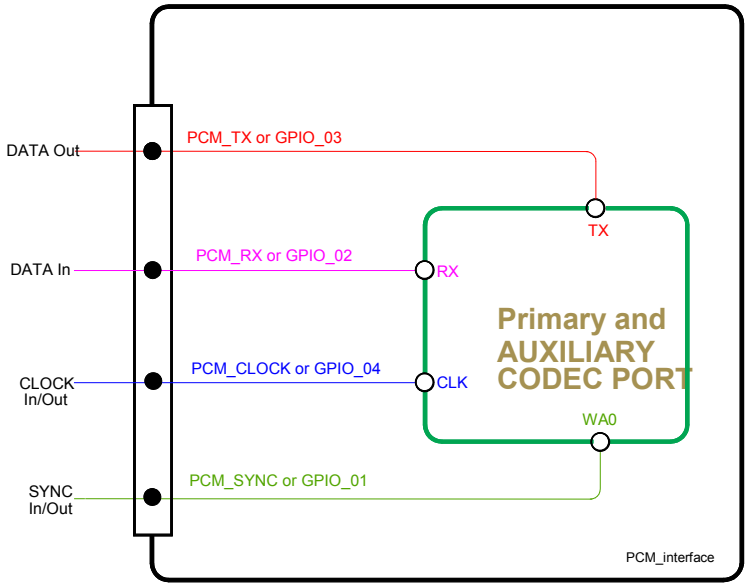


Figure 3.1 Primary and Auxiliary Codec Port signals routing

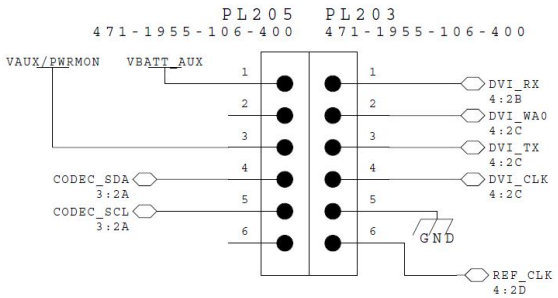
3.4.1 Pin position on UE/HE910V2_DE/CE910_HE920_CL865 Interface

Telit offers the dedicated Interface Board ***CS1467x, KS0145x and CS1531x*** where the **UE/HE910V2_DE/CE910_HE920_CL865** could be fitted on during the development phase of the customer application.

In such a way the useful signals are easily available on the connectors named PL203, PL102 and PL106.

DVI Function	PL203
DVI_CLK	**4**
DVI_WA0	**2**
DVI_RX	**1**
DVI_TX	**3**

Table 3.3 DVI signals Pin assignment on CS1467x for xE910-xxx



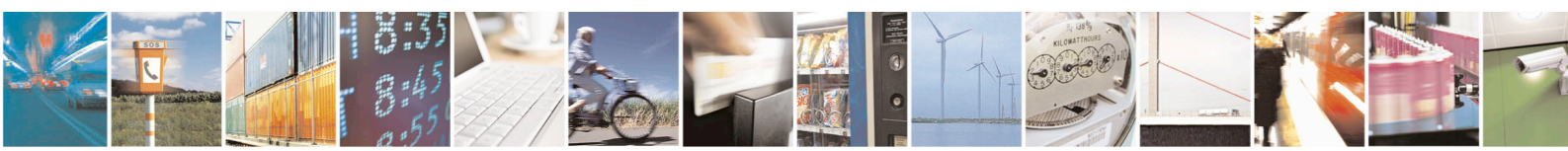


Figure 3.2 DVI Pin displacement on CS1467x for xE910-xxx

DVI Function	PL102
DVI_CLK	**4**
DVI_WA0	**3**
DVI_RX	**1**
DVI_TX	**2**

Table 3.4 DVI signals Pin assignment on KS0145x for xE920-xxx

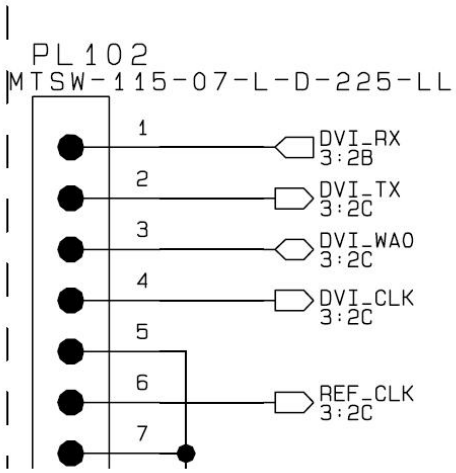


Figure 3.3 DVI Pin displacement on KS0145x for xE920-xxx

DVI Function	PL106
GPIO_04/DVI_CLK	**8**
GPIO_01/DVI_WA0	**4**
GPIO_02/DVI_RX	**2**
GPIO_03/DVI_TX	**6**

Table 3.6 DVI signals Pin assignment on CS1531x for CL865-xxx

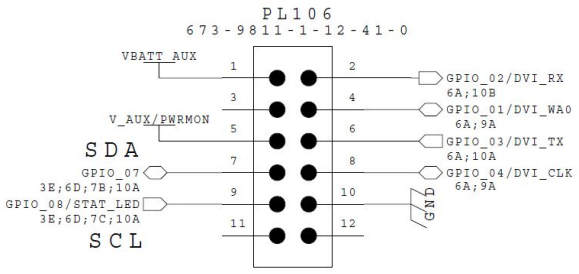
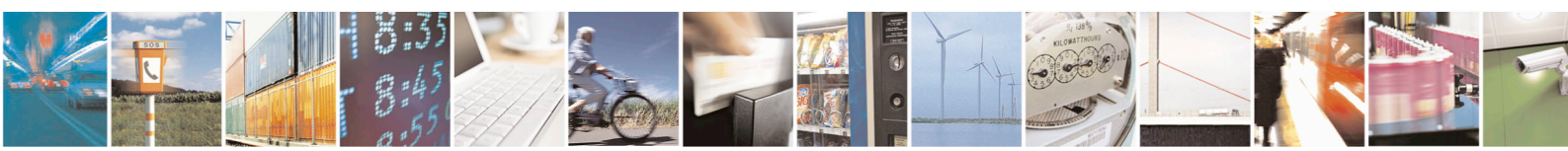


Figure 3.5 DVI Pin displacement on CS1531x for CL865-xxx



3.5 Electrical Characteristics

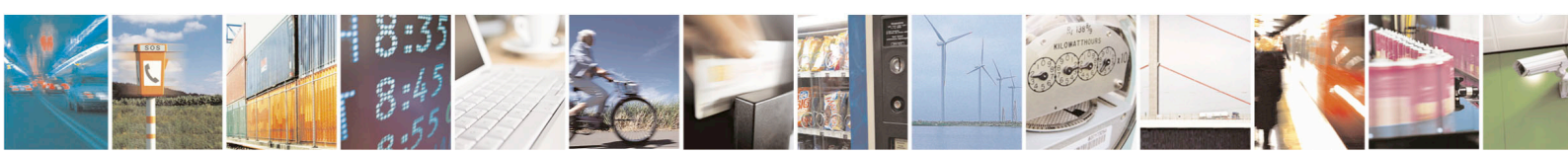
	Minimum	Maximum	Unit
V_{IL}	-0.3	0.36	V
V_{IH}	1.44	2.1	V
V_{OL}	-0.3	0.18	V
V_{OH}	1.62	2.1	V

Table 3.7 DVI signals Electrical characteristics for xE910-xxx, xE920-xxx and CL865-xxx

3.6 Clock and Sync direction

The table below summarizes how change the *Data Clock* and *Frame Synchronism* direction according to *Configuration Mode*.

				Master	Slave
Function	Name	Function		Direction	
PCM_CLOCK	***DVI_CLK***	**Data Clock**	→	**OUT**	**IN**
PCM_SYNC	***DVI_WA0***	**Frame Synchronism**	→	**OUT**	**IN**
PCM_RX	*DVI_RX*	Received Data	→	IN	IN
PCM_TX	*DVI_TX*	Transmitted Data	→	OUT	OUT



4 Protocol Description

The ***DVI*** operates in 16-bit data burst mode, starting with the most significant bit.

GSM voice is 13-bit *2's* complement but the output of the speech decoder is saved on 16-bit *2's* complement (Q15 format). The last 3 LSBs are equal to 0.

The frame lasts for 17 clock pulses, as one more clock pulse is needed for the frame synchronization of the signal ***PCM_SYNC***.

Following the falling edge of the ***PCM_SYNC*** signal, the data bits are sampled at the module data input (RX) and module output data (TX) at the next falling clock (CLK) pulse edge.

All data is 8 kHz and 16 bits with DVI (PCM interface).

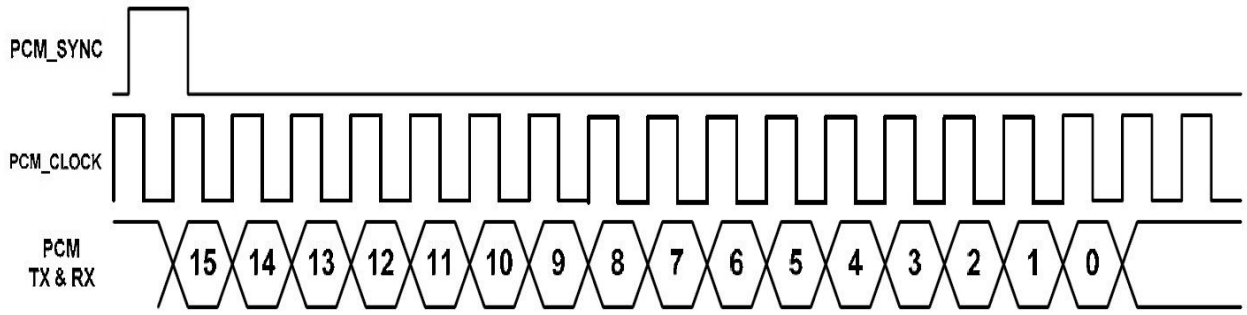
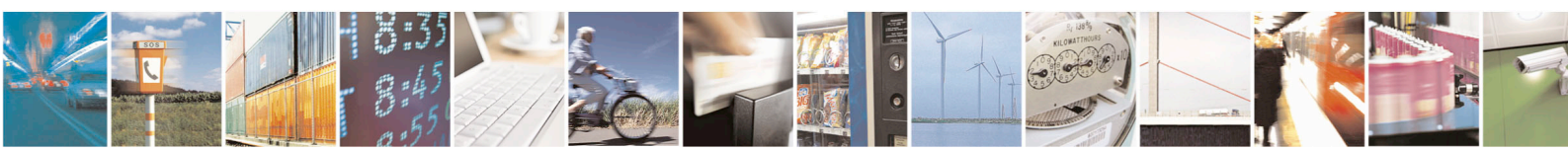


Figure 4.1 Digital Voice Interface (PCM) signal timing

4.1 Primary Mode

On ***Primary*** mode UE/HE910V2_DE/CE910_HE920_CL865 provide a 16-bit linear or 8-bit A-law or µ-law with padding, with short-sync and 2.048MHz clock (on the ***PCM_CLOCK*** pin).

Both ***Master*** and ***Slave*** mode are allowed.



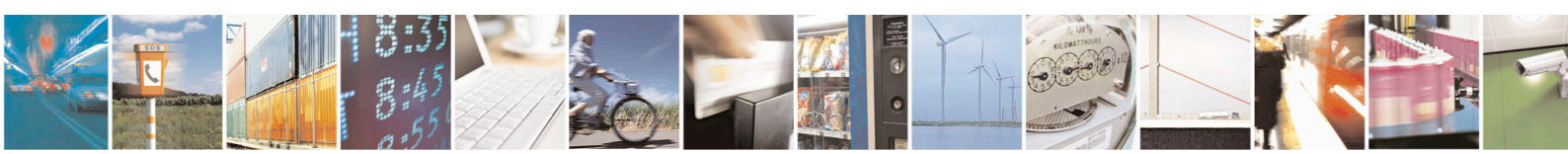
4.2 Auxiliary Mode

On ***Auxiliary mode*** UE/HE910V2_DE/CE910_HE920_CL865 provide 16-bit linear or 8-bit A-law or µ-law with padding, with ***long-sync*** and 128 KHz clock (on the **PCM_CLOCK** pin).

Only ***Master*** mode is allowed.

NOTE:

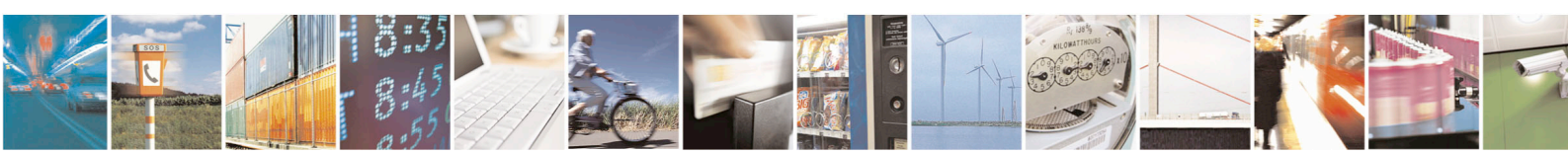
UE910-xxx DOES NOT support Auxiliary Mode (128K / Long-sync).



5 Parameters and Timing Characteristics

5.1 Primary PCM Interface

Parameter	Description	Min	Typical	Max	Units
t(sync)	PCM_SYNC cycle time		125		us
t(synch)	PCM_SYNC high time	400	500		ns
t(syncl)	PCM_SYNC low time		124.5		us
t(clk)	PCM_CLOCK cycle time		488		ns
t(clkh)	PCM_CLOCK high time		244		ns
t(clkl)	PCM_CLOCK low time		244		ns
t(susync)	PCM_SYNC setup time high before falling edge of PCM_CLOCK	60			ns
t(hsync)	PCM_SYNC hold time after falling edge of PCM_CLOCK	60			ns
t(sudin)	PCM_RX setup time before falling edge of PCM_CLOCK	50			ns
t(hdin)	PCM_RX hold time after falling edge of PCM_CLOCK	10			ns
t(pdout)	Delay from PCM_CLOCK rising to PCM_TX valid			350	ns
t(zdout)	Delay from PCM_CLOCK falling to PCM_TX HIGH-Z		160		ns



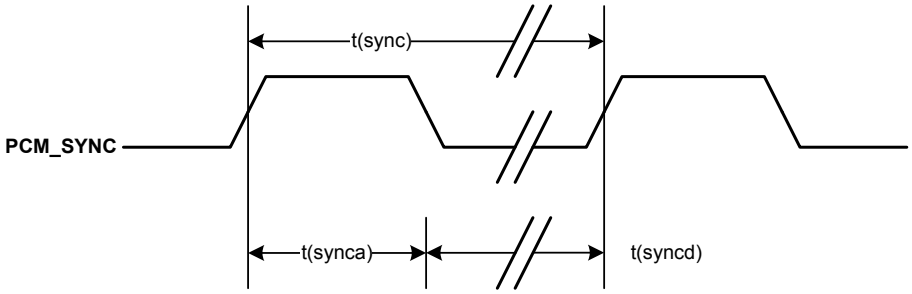


Figure 5.1 Primary PCM_SYNC timing (only Short sync)

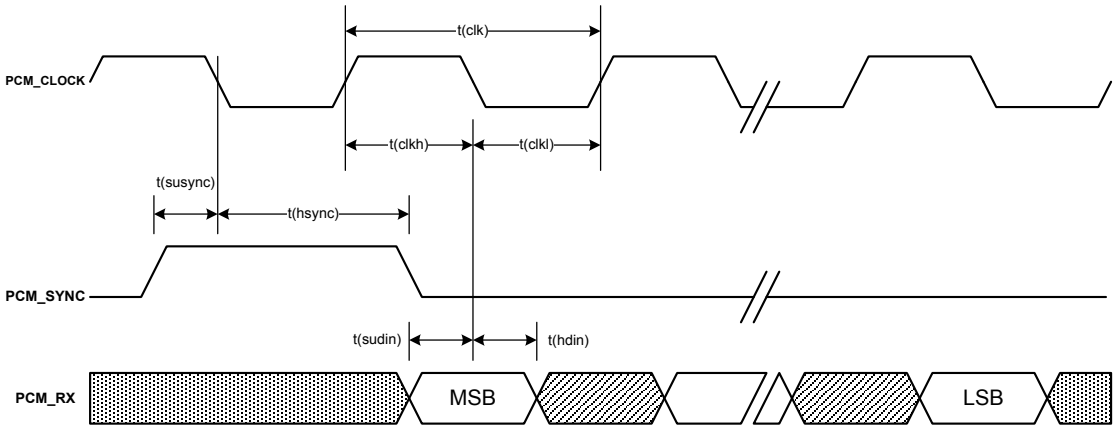


Figure 5.2 External codec to UE/HE910V2_DE/CE910_HE920_CL865 timing

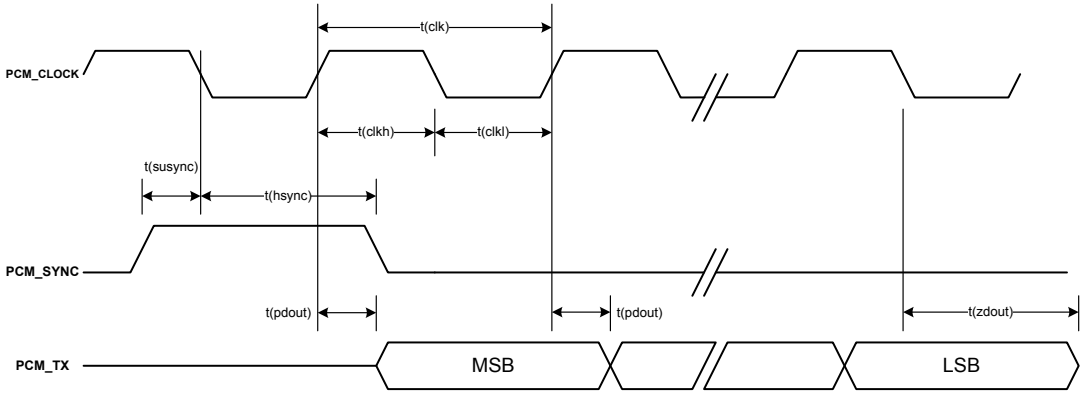
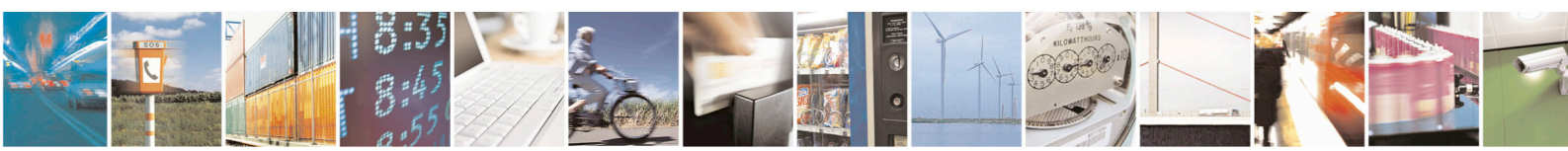


Figure 5.3 UE/HE910V2_DE/CE910_HE920_CL865 to External codec timing



5.2 Auxiliary PCM Interface

Parameter	Description	Min	Typical	Max	Units
t(auxsync)	PCM_SYNC cycle time		125		us
t(auxsynch)	PCM_SYNC high time	62.4	62.5		us
t(auxsyncl)	PCM_SYNC low time	62.4	62.5		us
t(auxclk)	PCM_CLOCK cycle time		7.8		us
t(auxclkh)	PCM_CLOCK high time	3.8	3.9		us
t(auxclkl)	PCM_CLOCK low time	3.8	3.9		us
t(suauxsync)	PCM_SYNC setup time high before falling edge of PCM_CLOCK	1.95			us
t(hauxsync)	PCM_SYNC hold time after falling edge of PCM_CLOCK	1.95			us
t(suauxdin)	PCM_RX setup time before falling edge of AUX_PCM_CLK	70			ns
t(hauxdin)	PCM_RX hold time after falling edge of AUX_PCM_CLK	20			ns
t(pauxdout)	Delay from AUX_PCM_CLK rising to AUX_PCM_TX valid			50	ns

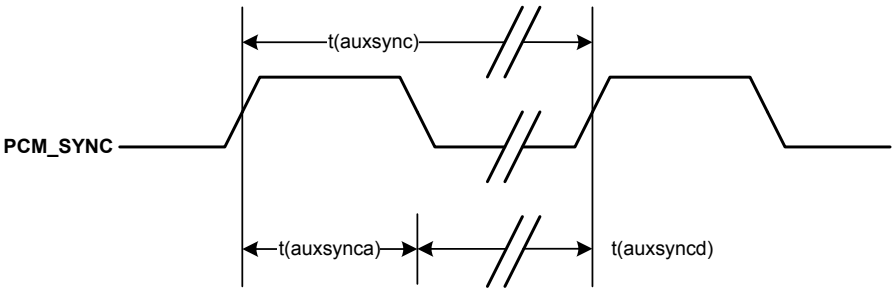


Figure 5.4 AUX PCM_SYNC timing (only Long sync)

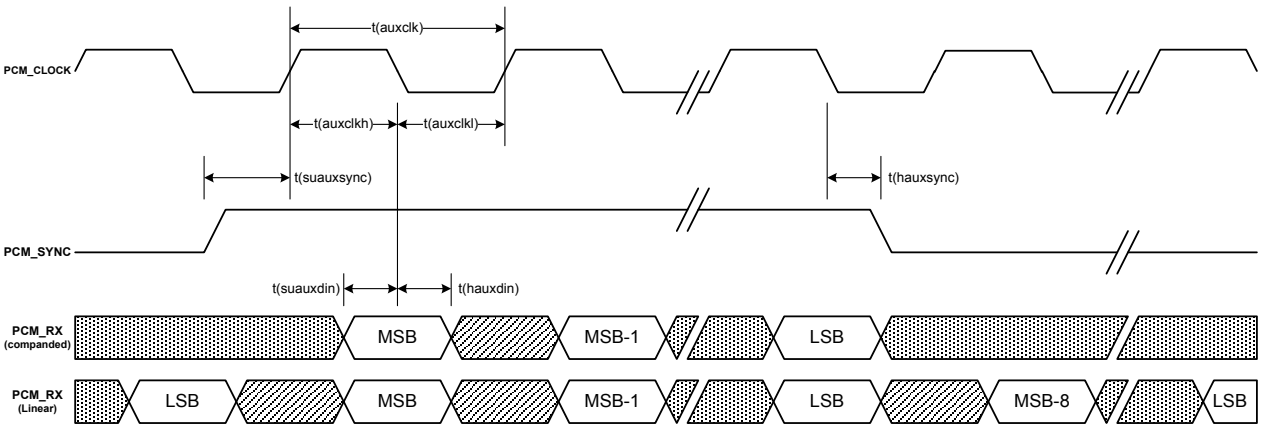
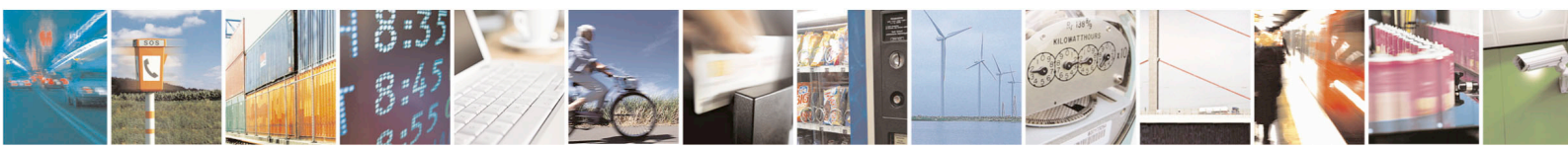


Figure 5.5 AUX External codec to UE/HE910V2_DE/CE910_HE920_CL865 timing



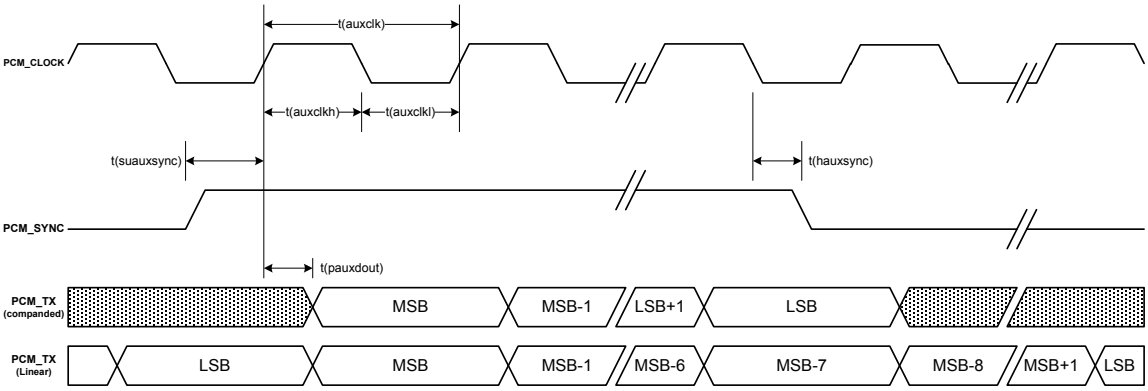
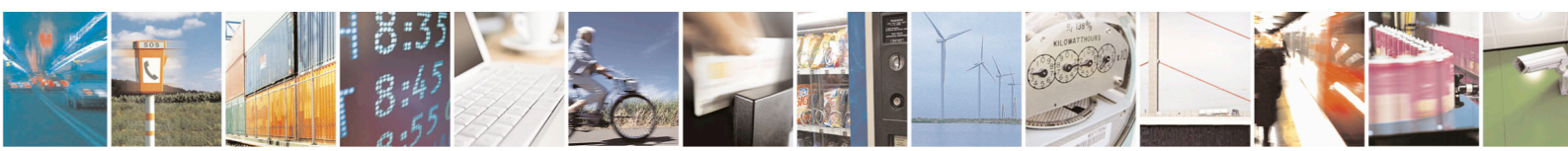


Figure 5.6 AUX UE/HE910V2_DE/CE910_HE920_CL865 to External codec timing

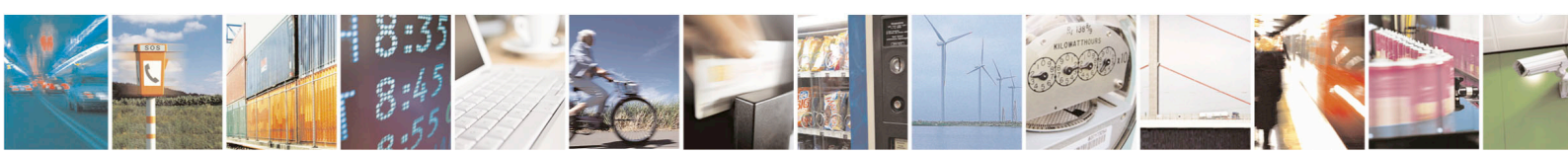


6 Custom AT Commands

The ***DVI can*** be set by the following custom ***AT commands***.
Needing more details, please refer to ***AT_Commands_Reference_Guide_<Model name>*** Telit specification document.

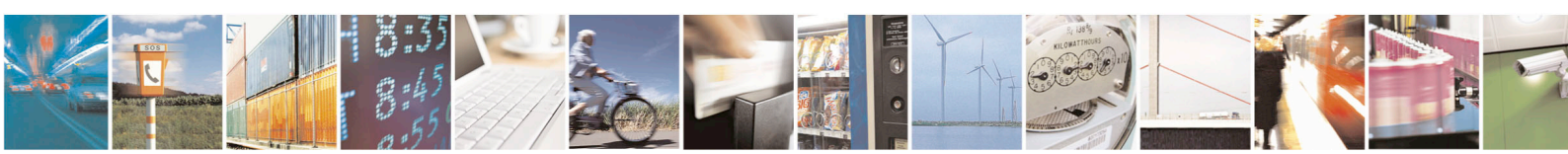
6.1 DVI port Enabling

#DVI - Digital Voiceband Interface	
AT#DVI=<mode> [,<dviport>, <clockmode>]	Set command enables/disables the Digital Voiceband Interface. Parameters: **<mode>** - enables/disables the DVI. 1 - enable DVI; audio is forwarded to the DVI block (factory default) **<dviport>** 2 - DVI port 2 will be used **<clockmode>** 0 - DVI slave 1 - DVI master (factory default) Note: **#DVI** parameters are saved in the extended profile
AT#DVI?	Read command reports last setting, in the format: **#DVI: <mode>,<dviport>,<clockmode>**
AT#DVI=?	Test command reports the range of supported values for parameters **<mode>,<dviport>** and **<clockmode>**
Example	AT#DVI=1,2,1 OK *DVI activated for audio. DVI is configured as master providing on DVI Port #2*



6.2 DVI port Configuration

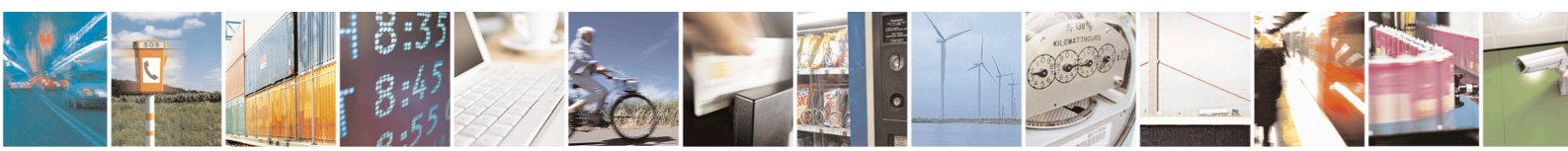
#DVICFG – DVI CONFIGURATION	
AT#DVICFG=[<clock>[,<decoder pad>[,<decoder format>[, <encoder pad>[,<encoder format>]]]]]	Set command sets the DVI configuration Parameter: **<clock>**: Clock speed for master mode 0 : normal mode 1 : high speed mode **<decoder pad>**: PCM padding enable in decoder path 0 : disable 1 : enable **<decoder format>**: PCM format in decoder path 0 : u-Law 1 : A-Law 2 : linear **<encoder pad>**: PCM padding enable in encoder path 0 : disable 1 : enable **<encoder format>**: PCM format in encoder path 0 : u-Law 1 : A-Law 2 : linear Note: #DVICFG parameters are saved in the extended profile
AT#DVICFG?	Read command reports the value of parameter in the format: **#DVICFG: <clock>,<decoder pad>,<decoder format>, <encoder pad>,<encoder format>**
AT#DVICFG=?	Test command returns the supported range of values of parameter **<clock>,<decoder pad>,<decoder format>, <encoder pad>,<encoder format>**.



6.3 DVI gain

#PCMTXG – DVI Microphone Gain	
AT#PCMTXG=<TX_VOL>	Set command sets the DVI (PCM) Audio TX gain Parameter: **<TX_VOL>** : PCM TX volume in TX path (factory default : 0) TX VOL RANGE : -5000(-50 dB) ~ 1200(+12 dB) Note: meaning of a TX_VOL is 1/100 dB step. Note: meaning of -50 dB is mute
AT#PCMTXG?	Read command returns the current PCM Audio TX value: **#PCMTXG: <TX_VOL>**
AT#PCMTXG=?	Test command returns the supported range of values of parameter **<TX_VOL>**

#PCMRXG – DVI Speaker Volume Level	
AT#PCMRXG=<RX_VOL>	Set command sets the PCM Audio RX value Parameter: **<RX_VOL>** : PCM RX volume in RX path (factory default : 0) RX_VOL RANGE : -5000(-50 dB) ~ 1200(+12 dB) Note: meaning of a RX_VOL is 1/100 dB step. Note: meaning of -50 dB is mute
AT#PCMRXG?	Read command returns the current PCM Audio RX value: **#PCMRXG: <RX VOL>**
AT#PCMRXG=?	Test command returns the supported range of values of parameter **<RX VOL>**

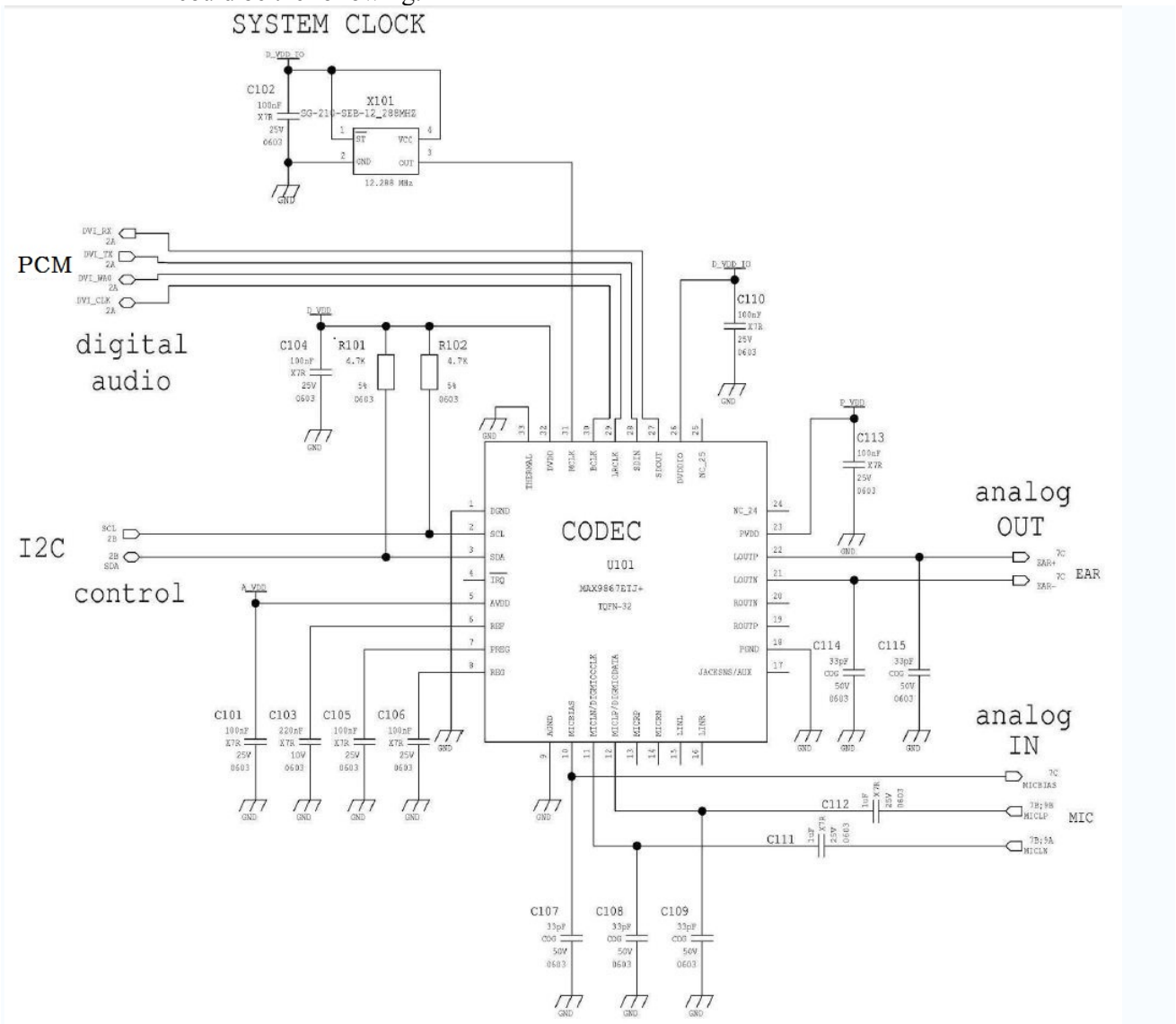


7 External Codec

The market offers great variety of audio codecs and, obviously, the customers will choose by itself the device that better fits their application.
Just as an example, in the following we go describing a possible interfacing with an external audio codec.

7.1 Schematic

A schematic example of an interface between the Telit's modules and the MAX9867 CODEC could be the following:



7.2 Codec and DVI settings

Speaker and microphone are connected to the external output input lines of the codec.
MAX9867 is configured by a script file, sent by a modem like Procomm® or Hyperlink®.
Every block defines some parameters to load:

- amplifiers gain
- signal mixing
- operating mode
- any other information needed

7.2.1 First step DVI signals routing

The DVI useful signals are routed to the assigned pin of the module.
Refer to the Telit module's HW User Guide for all information on the used DVI signals.

- DVI_TX, DVI_RX, DVI_WA0 and DVI_CLK

7.2.2 Second step DVI configuration

- Clock rate =2.048 MHz
- PCM decoder padding on
- decoder linear
- PCM encoder padding on
- Encoder linear

at command "AT#DVICFG=1,1,2,1,2

7.2.3 Last step DVI Activation and clock mode setting

- Enable DVI: audio is forwarded to the DVI block
- DVI port 4 will be used
- Clock mode DVI master

at command "AT#DVI=1,2,1^M"